EEEN301 Assignment 1

Due: midnight the 16th of April 2023

Total marks: 125 Marks

Please submit via the ECS online submission system.

Q1: Describe Moore's law. [2 marks]

Q2: Describe the difference between a 'microprocessor' and a SOC. [2 marks]

Q3: List 4 typical logical blocks that a SOC may have. [2 marks]

Q4: Describe what a cache is and explain the key principle how it can improve the performance of a microprocessor. [4 marks]

Q5: What is JTAG? Describe the different ways that we used it in the lab. [4 marks]

Q6: Discuss why chip designers prefer to use industry standard interfaces. [2 marks]

Q7: Discuss why some ARM processors have both the standard ARM instruction set as well as the Thumb instruction set. [4 marks]

Q8: Describe, in your own words, what steps the ARM processor performs to handle an IRQ exception. [6 marks]

Q9: Discuss why you may use a series of microprocessors in a product rather than just a single high performance one. [2 marks]

Q10: Describe what the link register 'LR' is and when it is typically used. [4 marks]

Q11: Describe the functions of the four most significant bits (MSB) of the CPSR register. [2 marks]

Q12: Convert the 8 bit number 0110 0000 to a negative two's complement number and then reverse it again. Show your working. [2 marks]

Q13: The register file is considered very fast memory. Why is it not used for all memory purposes? Justify your answer. [2 marks]

Q14: How is the address in a jump instruction treated to create a valid 32 bit address. [2 marks]

Q15: Provide the formats of R-type and I-type instructions. Explain how opcode is used. [2 marks]

Q16: Provide the instruction type, assembly language instruction, and binary representation of instruction described by the following LEGv8 fields: [2 marks]

```
op=0x658, Rm=13, Rn=15, Rd=17, shamt=0
```

Q17: Determine the assembly language instruction equivalent for the 32bit instruction value: 1000 1011 0001 0111 0000 0010 1000 1011. [2 marks]

Q18: Describe the function of an assembler and disassembler. [2 marks]

Q19: Describe the key difference between 'memory' and 'register' operands. [2 marks]

Q20: Describe why we prefer to use 'register' instructions as much as possible. [2 marks]

Q21: What is 'LSL' commonly used for? [2 marks]

Q22: What is 'masking' and how is it normally performed? [2 marks]

Q23: Describe the typical process of calling a procedure and what you need to consider [4 marks]

Q24: What addressing mode is used when implementing arrays in C [2 marks]

Q25: What addressing mode is used with branch instructions [2 marks]

Q26: Translate the following loop into C. Assume that the C-level integer *i* is held in register X10. X0 holds the C-level integer called result, and X1 holds the base address of the integer MemArray. [4 marks]

```
       ORR X10, XZR, XZR
LOOP: LDUR X11, [X1, #0]
       ADD X0, X0, X11
       ADDI X1, X1, #8
       ADDI X10, X10, #1
       CMPI X10, 100
       B.LT LOOP
```

Q27: Describe a way how we can manage a shared resource between two or more processor cores [4 marks]

Q28: Describe the key logic blocks that you would expect to find in a microprocessor [4 marks]

Q29: Describe 3 uses of the ALU logic block [3 marks]

Q30: What is the clock period? What is the clock rate? [2 marks]

Q31: Describe what typically limits the clock rate [2 marks]

Q32: Describe the key principle of pipelining and how it can improve performance. [2 marks]

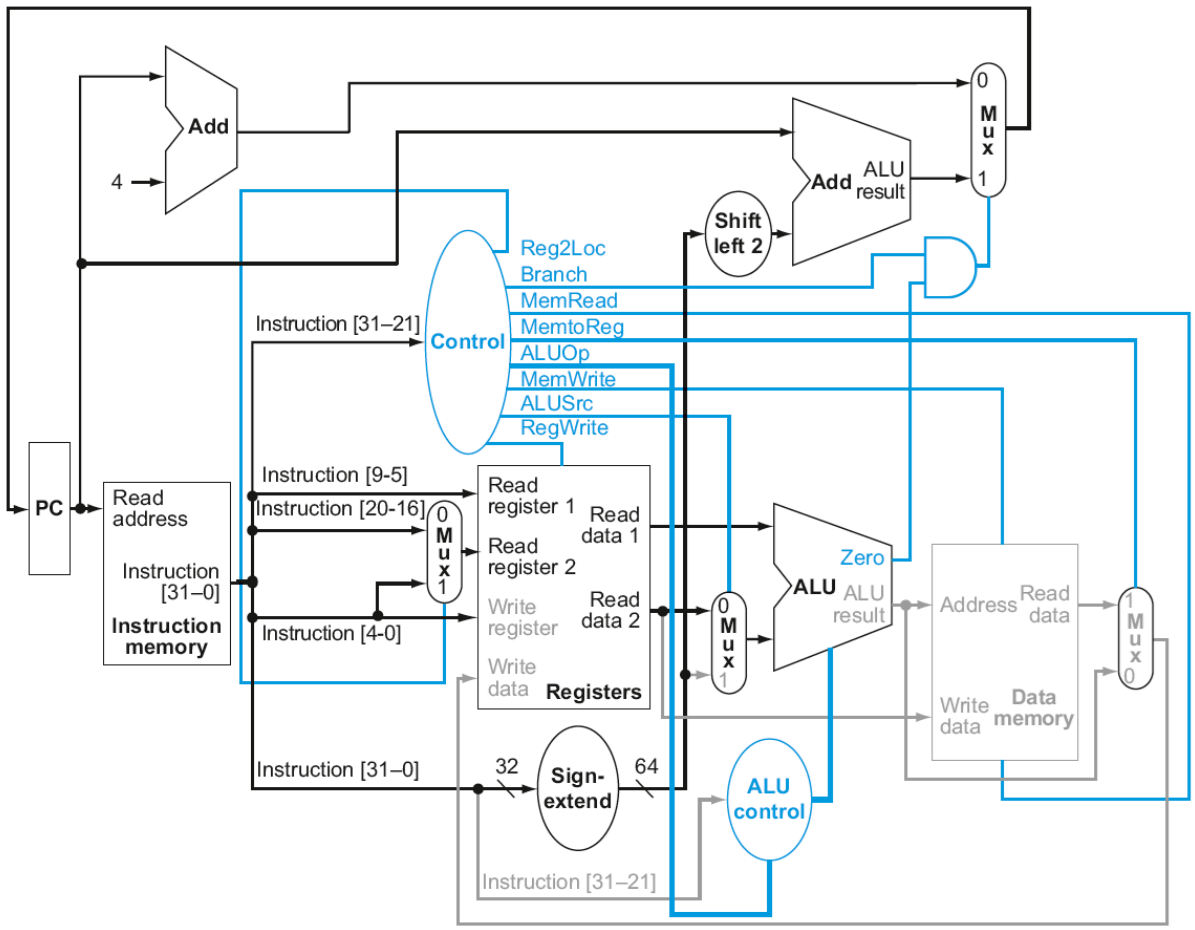
Q33: Describe at least two strategies that we can use to save power in a computer. [2 marks]

Q34: Describe how each of the following can affect program performance: [8 marks]

a. Your code
b. The compiler
c. The CPU
d. The I/O subsystem

Q35: Briefly describe the key "architecture" feature of each of these types of technologies: DSP, GPU, FPGA. [6 marks]

Q36: With reference to the diagram below, determine the logic levels of the control bits and then describe how the CBZ instruction is executed.



[8 marks]

Q37: Suppose you have a machine which executes a program that consists of 50% (in terms of execution time) floating point multiply, 20% floating point divide, and the remaining 30% are from other instructions.

(a) Management wants the machine to run 1.4 times faster. You can make the divide run at most 3 times faster and the multiply run at most 8 times faster. Can you meet the management's goal by making only one improvement, and which one? (Show the calculations you did to answer this question.) [4 marks]

(b) If you make both the multiply and divide improvements, what is the speed (performance) of the improved machine relative to the original machine? (Show the calculations you did to answer this question.) [3 marks]

Q38: Consider three different processors P1, P2, and P3 that support the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

(a) Which processor has the highest performance expressed in instructions per second? Show your calculations. [3 marks]

(b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions for each processor. [3 marks]

(c) We are trying to reduce the execution time by 30% (i.e., execution time is reduced from 10 seconds to 7 seconds). However, this leads to an increase of 20% in the CPI. For each processor, what clock rate should we have to get this time reduction? (Show the calculations you did to answer this question.) [3 marks]