School of
Engineering and Computer Science
Te Kura Mātai Pūkaha, Pūrorohiko

Prescription

Fundamentals of IC processing. Transistor based logic design using gates and switches, nMOS, CMOS, GaAs MESFET, BiCMOS logic design. Combinatoric arrays, sequential design, memory architectures, design for testability and observability. VLSI design using FPGAs.

Course learning objectives

Students who pass this course will be able to:

1. Fully understand how a FET operates over all its different modes of operation, and especially how FETs are employed in the construction of logic gates. (BE graduate attribute 3(a)). This is assessed via quizzes, written assignments, test and final examination.
2. Appreciate the different integrated chip technologies and be able to choose the best solution for a particular engineering problem. Technologies discussed in the course include Full Custom, SCA, MGA, FPGA, CPLD, PLA. (BE graduate attribute 3(b)). This is assessed via quizzes, written assignments, test and final examination.
3. Be able to implement a complex digital circuit in an FPGA using a variety of entry techniques including VHDL. (BE graduate attribute 3(f)). This is assessed via a practical and a written laboratory exercise.
4. Understand embedded circuit limitations and be able to employ techniques to improve testability and optimise designs. BE graduate attribute 3(b)). This is assessed via quizzes, written assignments, test and final examination.

Withdrawal from Course

Withdrawal dates and process:
https://www.victoria.ac.nz/students/study/course-additions-withdrawals

Lecturers

Robin Dykstra (Coordinator)

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Dale Carnegie

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224 Alan MacDiarmid Building, Kelburn

Teaching Format

There are two lectures each week.

Tutorials will be held most weeks to review assessment material, reinforce lecture content and answer specific student queries. The first four or five tutorial sessions will cover the VHDL design and several of these may be practical tutorials held in the lab. You should review the Tutorial material BEFORE attending the labs.

The course includes nine 3-hour assigned laboratory experiments. Four hours are assigned to each laboratory session to cater for students who have to miss an hour because of a lecture clash.

Student feedback

Student feedback on University courses may be found at:
www.cad.vuw.ac.nz/feedback/feedback_display.php

Dates (trimester, teaching & break dates)

- Teaching: 08 July 2019 - 13 October 2019
- Break: 19 August 2019 - 01 September 2019
- Study period: 14 October 2019 - 17 October 2019
- Exam period: 18 October 2019 - 09 November 2019

Class Times and Room Numbers

08 July 2019 - 18 August 2019

- **Monday** 14:10 - 15:00 – 118, Cotton, Kelburn
- **Wednesday** 14:10 - 16:00 – 119, Cotton, Kelburn

02 September 2019 - 13 October 2019

- **Monday** 14:10 - 15:00 – 118, Cotton, Kelburn
- **Wednesday** 14:10 - 16:00 – 119, Cotton, Kelburn

Other Classes

Laboratory sessions will be scheduled in the first week of term and will commence in the second week. The laboratory sessions will be held in CO239.

Set Texts and Recommended Readings

Required

Students will be provided with a comprehensive study guide which contains lecture slides but with blanks that will need to be filled-in during the lectures. A complete PDF file of these slides is available via BlackBoard for students who have either missed the lecture or wish to have the material entered in advance. The study-guide also includes sections of full notes. These sections have been included for those topics that are not well covered by the available text books. Additional material will be handed out in class and made available electronically.

A laboratory manual with the laboratory exercises and VHDL tutorial is also provided.

Recommended

The following texts contain information that would be useful to assist you in following the lecture material:

- Weste, N.H.E., and Harris, D., "*CMOS VLSI Design – A Circuits and Systems Perspective*", 3rd edition, Addison Wesley.
- Wolf, W., "*Modern VLSI Design, System-on-Chip Design*" 3rd edition, Prentice Hall.
- Weste, N., and Eshraghian, K., *Principles of CMOS VLSI Design – A Systems Perspective*, Addison Wesley.
- Jasinski, R., "*Effective Coding with VHDL*".

Mandatory Course Requirements

In addition to achieving an overall pass mark of at least 50%, students must:

- Satisfactorily completes at least 8 of the 10 assigned labs (a demonstrator must verify all lab work).
- Sit both of the 2 assigned internal tests
- Submit at least 2 assignments

If you believe that exceptional circumstances may prevent you from meeting the mandatory course requirements, contact the Course Coordinator for advice as soon as possible.

Assessment

This course has two one hour tests that will contribute 50% of the final grade. The internal course assessment comprises 15% written assignments, 10% mini-tests and 25% laboratory work, detailed below

Assessment Item	Due Date or Test Date	CLO(s)	Percentage
internal tests	Week 8 and 12	CLO: 1,2,3,4	50%
closed book mini-tests administered during lecture time	fortnightly	CLO: 1,2,3,4	10%
three internal written assignments		CLO: 1,2,3,4	15%
laboratory work including laboratory write-ups and mini project		CLO: 1,2,3,4	25%

Penalties

Late assessment is penalised at a rate of 5% per day the assessment is late.

Extensions

Individual extensions will only be granted in exceptional personal circumstances, and should be negotiated with the course coordinator before the deadline whenever possible. Documentation (eg, medical certificate) may be required.

Submission & Return

Lab work is submitted through the ECS submission system, accessible through the course web pages. Marks and comments will be returned through the ECS marking system, also available through the course web pages.

Marking Criteria

You are required to submit a formal laboratory report for each of the assigned labs. These should be of professional standard detailing the objective of the laboratory exercise, the methodology employed, justification for any design decisions, results obtained and an analysis or evaluation of your results. You should answer any questions asked of you in the laboratory manual.

Note, there is a non-linear relationship between the write-up mark and your overall laboratory grade. For example, a mark of 8/10 for a write-up certainly does not guarantee you an A grade for the laboratory work since several of these lab assessments are designated as mastery assessment items. This will be further explained in the lectures.

Group Work

We encourage you to discuss the principles of the course and assignments with other students, to help and seek help with programming details, problems involving the lab machines. However, any work you hand in must be your own work.

Workload

The expectation is that you will do roughly 10 hours of work per week on average. This will normally comprise 2 hours of lectures, 1 hour tutorial, 3 – 4 hours of laboratory work, and an average of 3 – 4 hours of assignment work, laboratory write-ups, and background reading.

Teaching Plan

The following material is expected to be covered during the lectures, although the exact order is expected to change with additional lectures being planned on FPGA design techniques. An approximate lecture schedule (excluding these changes) is as follows:

Week 0

Lecture	Introduction Overview
Lecture	FETS and Logic I FET operation
Lecture	FETS and Logic II FET operation, logic gate construction
Lecture	FETS and Logic III nMOS and CMOS logic gates
Lecture	FPGA I Introduction to FPGA
Lecture	FPGA II VHDL
Lecture	FPGA III Vivado
Lecture	FPGA IV Testbench design and IP block design
Lecture	Electrical Properties of nMOS I nMOS current equations
Lecture	Electrical Properties of nMOS II nMOS ratio calculations, nMOS parameters
Lecture	Electrical Properties of CMOS I CMOS regions and behaviour
Lecture	Electrical Properties of CMOS II CMOS and BiCMOS parameters
Lecture	CMOS & nMOS Design I Stick diagrams
Lecture	CMOS & nMOS Design II Design rules and memory
Test	TEST 1 Covers lectures 1 - 12 inclusive
Lecture	Basic Circuit Concepts I Sheet resistance, capacitance
Lecture	Basic Circuit Concepts II Scaling/optimisation
Lecture	VLSI Design Considerations I Gate vs switch logic, design issues
Lecture	VLSI Design Considerations II Packaging and power dissipation
Lecture	Reliability and Testing I Reliability measures, testing techniques
Lecture	Reliability and Testing II Testing techniques, design for testability

	Lecture	FPGA VI High level design
	Lecture	FPGA VII High speed design
	Test	TEST 2 Covers lectures 12 – 24 inclusive

Communication of Additional Information

Any additional information regarding this course will be posted on blackboard.

Links to General Course Information

- Academic Integrity and Plagiarism: https://www.victoria.ac.nz/students/study/exams/integrity-plagiarism
- Academic Progress: https://www.victoria.ac.nz/students/study/progress/academic-progess (including restrictions and non-engagement)
- Dates and deadlines: https://www.victoria.ac.nz/students/study/dates
- Grades: https://www.victoria.ac.nz/students/study/progress/grades
- Special passes: Refer to the Assessment Handbook, at https://www.victoria.ac.nz/documents/policy/staff-policy/assessment-handbook.pdf
- Statutes and policies, e.g. Student Conduct Statute: https://www.victoria.ac.nz/about/governance/strategy
- Student support: https://www.victoria.ac.nz/students/support
- Students with disabilities: https://www.victoria.ac.nz/st_services/disability/
- Student Charter: https://www.victoria.ac.nz/learning-teaching/learning-partnerships/student-charter
- Terms and Conditions: https://www.victoria.ac.nz/study/apply-enrol/terms-conditions/student-contract
- Turnitin: http://www.cad.vuw.ac.nz/wiki/index.php/Turnitin
- University structure: https://www.victoria.ac.nz/about/governance/structure
- VUWSA: http://www.vuwsa.org.nz

Offering CRN: 18513

Points: 15
Prerequisites: ECEN 202 (or PHYS 234), ECEN 204
Duration: 08 July 2019 - 10 November 2019
Starts: Trimester 2
Campus: Kelburn