School of
Engineering and Computer Science
Te Kura Mātai Pūkaha, Pūrorohiko

Prescription

A practically oriented introduction to the design and construction of digital electronic instruments. The course provides a foundation in binary arithmetic and Boolean algebra, logic gates and families, combinational and sequential logic design, microprocessor architectures, programming and interfacing, and conversions of digital and analogue signals.

Course learning objectives

Students who pass this course will be able to:

1. Describe the properties, construction and operating characteristics of digital integrated circuits from the most important CMOS Logic families. (BE graduate attribute 3(a))
2. Describe the basic logic operations using Boolean algebra, truth tables and logic circuits and be able to simplify complex combinatorial logic circuits via Boolean algebra and the Karnaugh map method. ((BE graduate attribute 3(a))
3. Understand the use of various types of flip-flops in creating sequential circuits and their uses in synchronisation, frequency division and counting. (BE graduate attribute 3(a,b))
4. Design synchronous sequential circuits. ((BE graduate attribute 3(b,c))
5. Understand the basic architecture of a microcontroller by using the 8051 microcontroller as an example ((BE graduate attribute 3(a))
6. Be able to program a microprocessor in assembly language. ((BE graduate attribute 3(a, b))
7. Be able to implement a real-world interfacing to a microprocessor. ((BE graduate attribute 3(a, b))

Withdrawal from Course

Withdrawal dates and process:
https://www.victoria.ac.nz/students/study/course-additions-withdrawals

Lecturers

Gideon Gouws (Coordinator)

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225 Alan MacDiarmid Building, Kelburn

Jim Murphy

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202 92 Fairlie Tce, Kelburn

Teaching Format

During the trimester there will be three lectures and a three hour lab per week.

Student feedback

Student feedback on University courses may be found at: www.cad.vuw.ac.nz/feedback/feedback_display.php

Dates (trimester, teaching & break dates)

- Teaching: 04 March 2019 - 09 June 2019
- Break: 15 April 2019 - 28 April 2019
- Study period: 10 June 2019 - 13 June 2019
- Exam period: 14 June 2019 - 29 June 2019

Class Times and Room Numbers

04 March 2019 - 14 April 2019

- **Tuesday** 13:10 - 14:00 – 202, New Kirk, Kelburn
- **Wednesday** 16:10 - 17:00 – 202, New Kirk, Kelburn
- **Thursday** 11:00 - 11:50 – 102, Alan MacDiarmid Building, Kelburn

29 April 2019 - 09 June 2019

- **Tuesday** 13:10 - 14:00 – 202, New Kirk, Kelburn
- **Wednesday** 16:10 - 17:00 – 202, New Kirk, Kelburn
- **Thursday** 11:00 - 11:50 – 102, Alan MacDiarmid Building, Kelburn

Other Classes

One 3-hour lab/week in LB217. Allocation of the lab sessions will take place in the first week and labs will start in week 2.

Set Texts and Recommended Readings

Required

The book "*Digital Systems*", by R J Tocci is the recommended text, but the book "*Electronics A Systems Approach*" by Storey may be used as additional reading. The library should have some copies on closed reserve and on 3 – day loan. Any edition from the 7th or later is suitable.

Mandatory Course Requirements

In addition to achieving an overall pass mark of at least 50%, students must:

- Satisfactory completion of at least 5 of the laboratory experiments.
- A minimum of 40% averaged over the two in-term tests.

If you believe that exceptional circumstances may prevent you from meeting the mandatory course

requirements, contact the Course Coordinator for advice as soon as possible.

Assessment

The assessment for ECEN 202 involves assignments, two in-term tests and weekly laboratories as detailed below.

Laboratory Work

The course has ten laboratory sessions associated with it. All experimental work must be started in the scheduled periods. If you do not complete the work in this session, arrangements can be made to complete at a later stage (before the next session). However, no laboratory demonstrators will be available out of sessions.

It is required that you keep detailed experimental notes for all experiments in a logbook. In addition, data acquired/graphs plotted should be electronically stored and kept to the end of the course. A 2B5 hardcover is ideal for this.

At the end of each laboratory you will be required to submit a short laboratory report. This report will be based on a number of questions asked at the end of each laboratory script. This report must be handed in no later than one week after the experiment had been scheduled.

Your final mark for each laboratory will consist of a mark for your report as well as a mark assigned by the lecturer/lab demonstrator for your contribution in the laboratory.

Assignments

Assignments will be set approximately once every two weeks and should be handed in before the required deadline.

Assessment Item	Due Date or Test Date	CLO(s)	Percentage
Laboratory Work	Weeks 2-11	CLO: 1,2,3,4,5,6	30%
Assignments	Weeks 2-12	CLO: 1,2,3,4,5	10%
Test 1	Week 6	CLO: 1,2,3	30%
Test 2	Week 12	CLO: 3,4,5	30%

Penalties

All work is due in on the due date. Marks will be deducted at a rate of 10% of the full mark for each working day late. Work will not be marked if more than 1 week late.

Extensions

Extensions must be requested in writing (email) and will only be given in exceptional circumstances, and if agreed before the due date. No late work will be accepted after the model solutions to any piece of assessment have been distributed to the class.

Submission & Return

Drop boxes on the second floor of the Laby building (outside the lab), will be marked for your laboratory reports or assignments.

Workload

In order to maintain satisfactory progress in ECEN 202, you should plan to spend an average of 10-12 hours per week on this paper, including during exam periods. A plausible and approximate breakdown for these hours would be:

Lectures and tutorials: 3 hours Labs: 3 hours
Assignments: 2 hours Readings: 2 hours

Teaching Plan

The following material will be covered during ECEN 202:

Overview of logic gates, combinatorial logic, Boolean algebra, simplification, K-maps
Properties of digital logic ICs
Sequential logic, Flip-Flops, Counters, asynchronous and synchronous,
Registers, Arithmetic Circuits
Design of synchronous counters, state machines
Selected Special Function Digital ICs
Microprocessor architecture and operation based on 8051,
Timing, polling and interrupts
Analog to digital conversion,
Introduction to sampling
Memory Devices

Communication of Additional Information

Course materials and other information will be available from https://ecs.victoria.ac.nz/Courses/ECEN202_2019T1/. Students should check there regularly.

Links to General Course Information

- Academic Integrity and Plagiarism: https://www.victoria.ac.nz/students/study/exams/integrity-plagiarism
- Academic Progress: https://www.victoria.ac.nz/students/study/progress/academic-progess (including restrictions and non-engagement)
- Dates and deadlines: https://www.victoria.ac.nz/students/study/dates
- Grades: https://www.victoria.ac.nz/students/study/progress/grades
- Special passes: Refer to the Assessment Handbook, at https://www.victoria.ac.nz/documents/policy/staff-policy/assessment-handbook.pdf
- Statutes and policies, e.g. Student Conduct Statute: https://www.victoria.ac.nz/about/governance/strategy
- Student support: https://www.victoria.ac.nz/students/support
- Students with disabilities: https://www.victoria.ac.nz/st_services/disability/
- Student Charter: https://www.victoria.ac.nz/learning-teaching/learning-partnerships/student-charter
- Terms and Conditions: https://www.victoria.ac.nz/study/apply-enrol/terms-conditions/student-contract
- Turnitin: http://www.cad.vuw.ac.nz/wiki/index.php/Turnitin
- University structure: https://www.victoria.ac.nz/about/governance/structure
- VUWSA: http://www.vuwsa.org.nz

Offering CRN: 18509

Points: 15
Prerequisites: ENGR 101 or PHYS 115; 15 pts from (ENGR 121, 122, 123, MATH 141, 142, 151, 161)
Restrictions: PHYS 234
Duration: 04 March 2019 - 30 June 2019
Starts: Trimester 1

Campus: Kelburn