

Integrated Digital Electronics - Course Outline

ECEN 302: 2012 Trimester 2

This document sets out the workload and assessment requirements for ECEN 302. It also provides contact information for staff involved in the course. If the contents of this document are altered during the course, you will be advised of the change by an announcement in lectures and/or on the course Blackboard site.

Objectives

By the end of the course, students should:

1. Fully understand how a FET operates over all its different modes of operation. This appreciation will include an understanding of gate capacitance, charge/discharge resistances, driving ability, circuit delays, dimensions, oxide thickness, limitations to speed and scaling, and how its performance differs from a similar sized BJT. The student will be able to quantitatively determine diffusion and oxidation times, diffusion and ion-implantation doses and times in order to achieve a desired IC fabrication parameter. ([BE graduate attribute 3\(a\)](#))
2. Appreciate the different integrated chip technologies and be able to choose the best solution for a particular engineering problem. Technologies discussed in the course include Full Custom, SCA, MGA, FPGA, CPLD, PLA. ([BE graduate attribute 3\(b\)](#))
3. Be able to implement large combinatorial, sequential and memory logic structures in an integrated digital chip. ([BE graduate attribute 3\(f\)](#))
4. Be able to implement a complex digital circuit in an FPGA using a variety of entry techniques including VHDL. ([BE graduate attribute 3\(f\)](#))
5. Be able to effectively communicate in a written manner the methodology, design compromises, results and evaluation of an FPGA implementation of a digital design. ([BE graduate attribute 2\(b\)](#))
6. Be able to effectively communicate the results of an analysis of various forms of digital implementation detailing a comparison of applicable technologies, their advantages and disadvantages. ([BE graduate attribute 2\(b\)](#))
7. Understand how digital circuits are constructed and the advantages/disadvantages of an nMOS, pMOS, CMOS, BJT and BiMOS implementations. ([BE graduate attribute 3\(b\)](#))
8. Understand how integrated circuits are designed and constructed and hence understand the fundamental limitations of scaling and the variability inherent in semiconductor manufacturing. To demonstrate this understanding a student should be able to design simple full-custom circuits using the λ based design rules. ([BE graduate attribute 3\(e\)](#))
9. Understand how different design architectures affect the speed and size of digital integrated designs. This understanding will be demonstrated by an ability to quantitatively calculate circuit speeds and to obtain a compromise design between speed, area, noise margins, and power dissipation. ([BE graduate attribute 3\(b\)](#))
10. Understand the issues of controllability and observability and be able to design for testability. ([BE graduate attribute 3\(f\)](#))
11. Be able to construct test vectors using the stuck-at fault model. ([BE graduate attribute 3\(f\)](#))
12. Understand and be able to quantify the issues involved in packaging, particular power distribution and heat dissipation. ([BE graduate attribute 3\(f\)](#))
13. Be able to understand and summarise literature available online and elsewhere in order to supplement the information provided during the lectures. Several assessment questions will require the student to undertake such independent research. ([BE graduate attribute 3\(d\)](#))

Prerequisites

The prerequisites for ECEN 302 are:

- ECEN202

Course Materials and Textbook

Students will be provided with a comprehensive study guide which contains all the lecture OHTs but with blanks that will need to be filled-in during the lectures. A complete PDF of these slides is available via Blackboard for students who have either missed a lecture or wish to have the material entered in advance. The study guide also includes sections of full notes. These sections have been included for those topics that are not covered by the available text books.

A laboratory manual with the laboratory exercises and VHDL tutorial is also provided.

The following texts contain information that would be useful to assist you in following the lecture material:

- Weste, N.H.E., and Harris, D., *CMOS VLSI Design – A Circuits and Systems Perspective*, 3rd edition, Addison Wesley.

Students may gain additional benefit from purchasing:

- Wolf, W., *Modern VLSI Design, System-on-Chip Design* 3rd edition, Prentice Hall.
- Weste, N., and Eshraghian, K., *Principles of CMOS VLSI Design – A Systems Perspective*, Addison Wesley.

Purchase of these texts is not required for 2012.

Lectures, Tutorials, Laboratories, and Practical work

A schedule of lecture topics is available online.

Lectures and tutorial sessions for ECEN 302 are:

- Monday 10:00 - 10:50 am in Laby LT118
- Thursday 1:10 - 3:00 pm in Laby LT118

Laboratory sessions will be scheduled in the first week of term and will commence in the second week. The laboratory sessions will be held in CO 249.

Tutorials will be held most weeks to review assessment material, reinforce lecture content and answer specific student queries. The first three or four lab sessions will also contain a tutorial element covering the VHDL design. You should review the tutorial BEFORE attending the lab.

Laboratories

The course includes nine 3-hour assigned laboratory experiments.

- **Laboratory Reports** You are required to submit a formal laboratory report for each of the assigned labs. These should be of professional standard detailing the objective of the laboratory exercise, the methodology employed, a justification for any design decisions, results obtained and an analysis or evaluation of your results. You should answer any questions asked of you in the laboratory manual.

Assessment

This course has a formal 3 hour exam that will contribute 50% of the final grade. The internal course assessment comprises 40% written assignments, 40% tests and mini-tests and 20% laboratory work, detailed as follows:

30%	internal test (on or about September 20)
10%	closed book mini-tests administered during lecture time
40%	three internal written assignments (equal weighting)
20%	laboratory work including laboratory write-ups and laboratory practical marks

Note there is a non-linear relationship between the write-up mark and your overall laboratory grade. For example, a mark of 8/10 for a write-up does not guarantee you an A grade for the laboratory work since several of these items are designated as mastery assignments. This will be further explained in the lectures.

Late assessment will be penalized at the rate of 5% per day the assessment is late.

Workload

The expectation is that you will do roughly 10 hours of work per week on average. This will normally comprise

- 2 hours of lectures
- 1 hour tutorial
- 3-4 hours of laboratory work, and
- on average 3-4 hours of assignment work, laboratory write-ups, and background reading.

School of Engineering and Computer Science

The School office is located on level three of the Cotton Building (Cotton 358).

Staff

The course coordinator and lecturer for ECEN 302 is Dale Carnegie. His contact details are:

- Dale Carnegie
- CO 342

- +64 4 463 7485
- Dale.Carnegie@vuw.ac.nz

A senior graduate student (Ben Drayton) will supervise the laboratory work. Ben's laboratory is Laby 311 (email b.drayton@gmail.com). He will (probably) be assisted by PhD student Henry Williams and Masters student Tony Cimino.

Announcements and Communication

This course uses Blackboard. Course materials and other information will be posted on Blackboard. Students should check Blackboard regularly.

Registered students will find information on Blackboard at: <http://blackboard.vuw.ac.nz>

Plagiarism

Working Together and Plagiarism

We encourage you to discuss the principles of the course and assignments with other students, to help and seek help with programming details, problems involving the lab machines. However, any work you hand in must be your own work.

The [School policy on Plagiarism](#) (claiming other people's work as your own) is available from the course home page. Please read it. We will penalise anyone we find plagiarising, whether from students currently doing the course, or from other sources. Students who knowingly allow other students to copy their work may also be penalised. If you have had help from someone else (other than a tutor), it is always safe to state the help that you got. For example, if you had help from someone else in writing a component of your code, it is not plagiarism as long as you state (eg, as a comment in the code) who helped you in writing the method.

Mandatory Requirements

It is expected that ALL work will be completed and handed in for marking. An incomplete or fail grade will be issued to any student who satisfies ANY of the below requirements.

1. Satisfactorily completes less than 7 of the 9 assigned labs (a demonstrator must verify all lab work). Note that sessions 3 & 4, and sessions 8 & 9 are double labs intended to take 2 weeks to complete. Failure to satisfactorily complete one of these double labs will count as two failures to this mandatory standard.
2. Does not turn up for the assigned internal test.
3. Hands in less than 3 assignments.
4. Is caught cheating in any form (this includes laboratory work)
5. Scores less than 35% in the final exam.

Passing ECEN 302

To pass ECEN 302, a student must satisfy mandatory requirements and gain at least a **C** grade overall.

Withdrawal

The last date for withdrawal from ECEN 302 with entitlement to a refund of tuition fees is Friday 27 July 2012. The last date for withdrawal without being regarded as having failed the course is Friday 28 Sept 2012 -- though later withdrawals may be approved by the Dean in special circumstances.

Rules & Policies

Find key dates, explanations of grades and other useful information at <http://www.victoria.ac.nz/home/study>.

Find out about academic progress and restricted enrolment at <http://www.victoria.ac.nz/home/study/academic-progress>.

The University's statutes and policies are available at <http://www.victoria.ac.nz/home/about/policy>, except qualification statutes, which are available via the Calendar webpage at <http://www.victoria.ac.nz/home/study/calendar> (See Section C).

Further information about the University's academic processes can be found on the website of the Assistant Vice-Chancellor (Academic) at <http://www.victoria.ac.nz/home/about/avcacademic>

All students are expected to be familiar with the following regulations and policies, which are available from the school web site:

[Grievances](#)

[Student and Staff Conduct](#)

[Meeting the Needs of Students with Disabilities](#)

[Student Support](#)

[Academic Integrity and Plagiarism](#)

[Dates and Deadlines including Withdrawal dates](#)

[School Laboratory Hours and Rules](#)

Printing Allocations
Expectations of Students in ECS courses

The School of Engineering and Computer Science strives to anticipate all problems associated with its courses, laboratories and equipment. We hope you will find that your courses meet your expectations of a quality learning experience.

If you think we have overlooked something or would like to make a suggestion feel free to talk to your course organiser or lecturer.
