ECEN (XMUT) 202
Digital Electronics

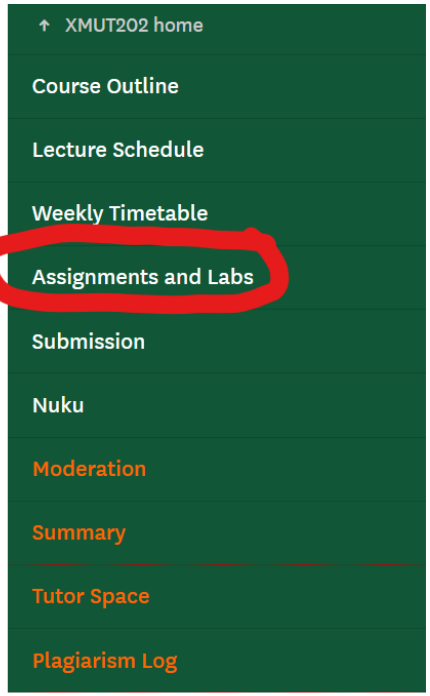
A/Prof. Pawel Dmochowski

School of Engineering and Computer Science
Victoria University of Wellington

Victoria
UNIVERSITY OF WELLINGTON
Te Whare Wānanga
o te Ūpoko o te Ika a Māui
CAPITAL CITY UNIVERSITY

Week 9 Lecture 1b

- Lab 4 Overview



School of Engineering and Computer Science ▸ Courses/XMUT202_2024T1 ▸ Assignments ▸ Lab4

Digital Electronics, XMUT 2024

Lab 4: Combinatorial Logic

Due 7 April , 19 pm (Xiamen Time)

Note: You must present your projects to co-teachers or tutors in the lab.

Resources and links:

- Lab4 Instructions
- Lab 4 Data Sheets:
  - 74HC_HCT00
  - 74HC_HCT02
  - 74HCT04
  - 74HC_HCT153

Logic Gates and Combinatorial Logic

1. Learning Objectives

The purpose of this lab is to:

a. serve as a review of the characteristics of basic logic gates.

b. allow the construction of basic digital circuits using a breadboard and design station

c. use the basic logic gates as combinatorial building blocks to synthesize complex logic functions.

d. use multiplexers to implement logic function

2 Introduction.

2.1 Building real logic circuits using integrated circuit logic gates

In this lab we will start to build logic circuits using digital integrated circuits (ICs). All the ICs we will use are based on CMOS (**c**omplementary **m**etal **o**xide **s**emiconductor) oxide technology. The technology and characteristics of these devices will be discussed in more detail in class. We will specifically use the 74HCT family of ICs, which makes them totally compatible with older TTL (transistor-transistor logic) devices. The IC number should normally look as follows:

AA 74HCT XXX B or in the simpler form 74HCTXXX.

This number can be decoded as follows:

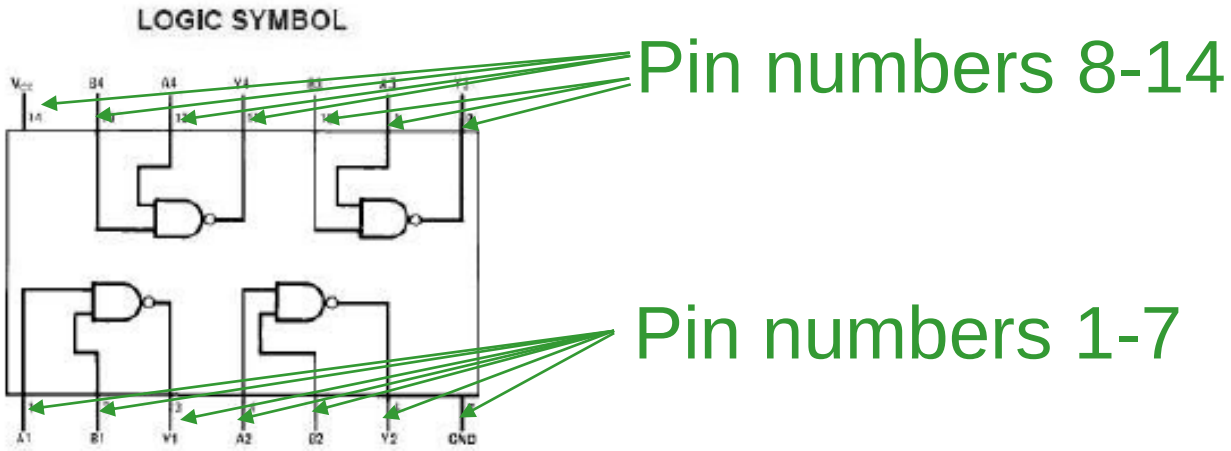
AA: Typically a two letter code that indicates the manufacturer

74 or 54: The temperature range over which the IC will work. Commercial devices (74) have a temperature range of typically 0 – 70 ^{o}C, while military specified devices (54) will have a temperature range of -55 to 125 ^{o}C.

B: The last part of the number may be a single letter that indicates the type of package of the device.

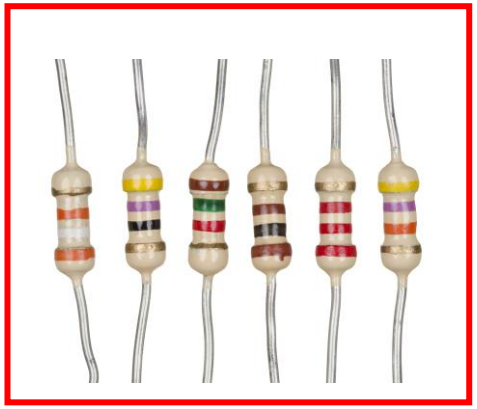
The logic gates that we use are designed as part of an integrated circuit, which is then packaged to produce an IC with typically 14 pins. These pins provide electrical connection between the external circuit and the internal logic gates. This enables multiple logic gates to be included on the same package and in the figure below the internal arrangement of a 74HCT00 CMOS NAND gate is shown. It can be seen that the internal structure consists of four two-input NAND gates, which thus needs twelve of the fourteen pins of the package. Of course the IC also needs power to enable these gates to work, and a power and ground is supplied in pins 14 and 7 respectively.

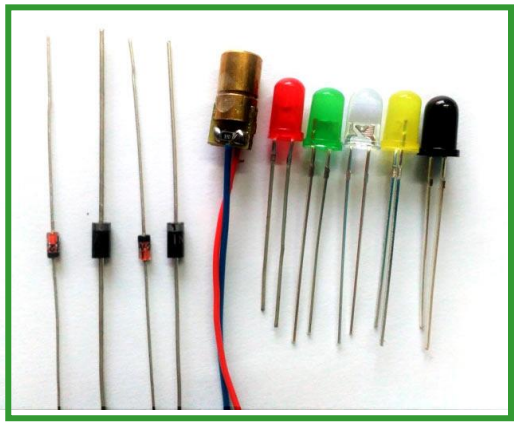
74HCT00 Quad 2-Input NAND Gate

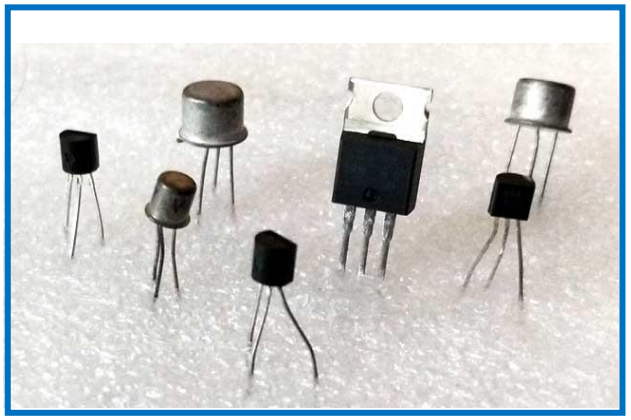


Basic Characteristics of ICs

Integrated Circuits (ICs or chips) is made up of resistors, diodes and transistors fabricated on a single piece of semiconductor



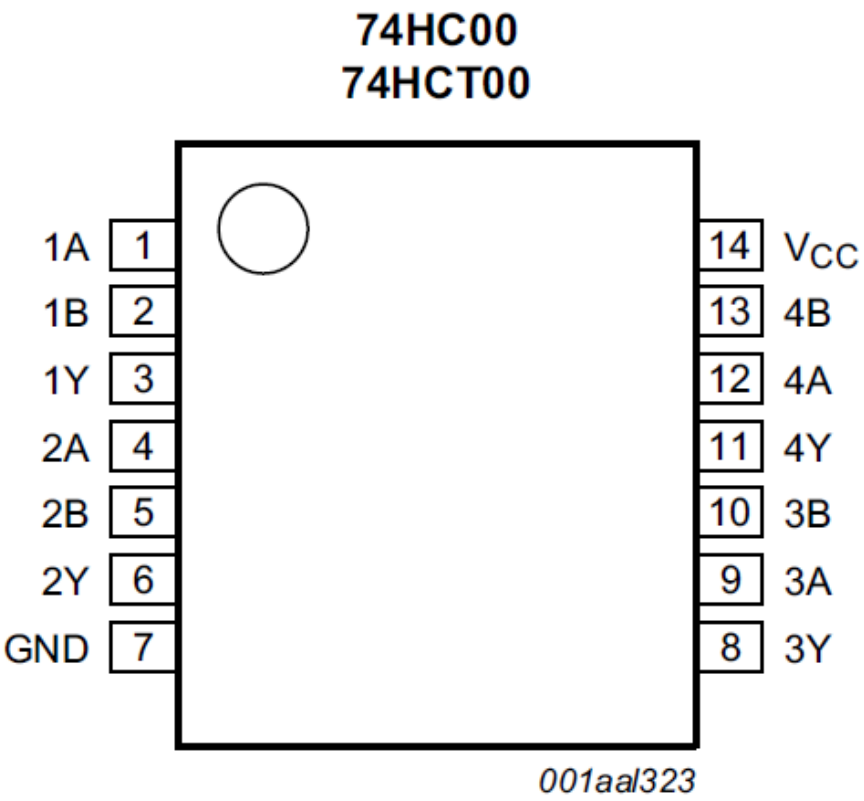




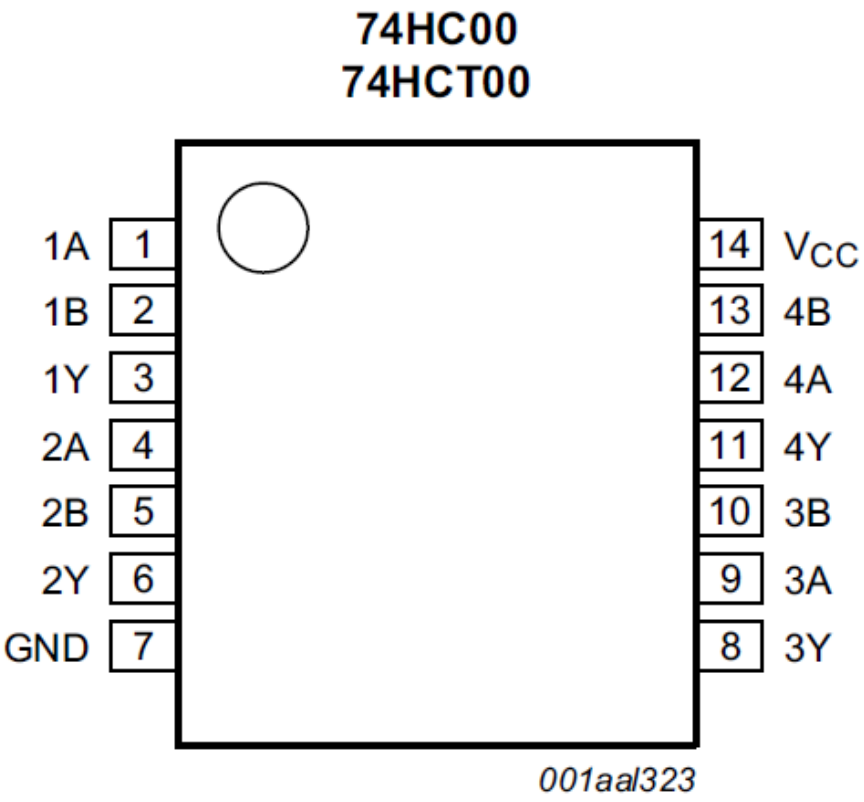
Basic Characteristics of ICs

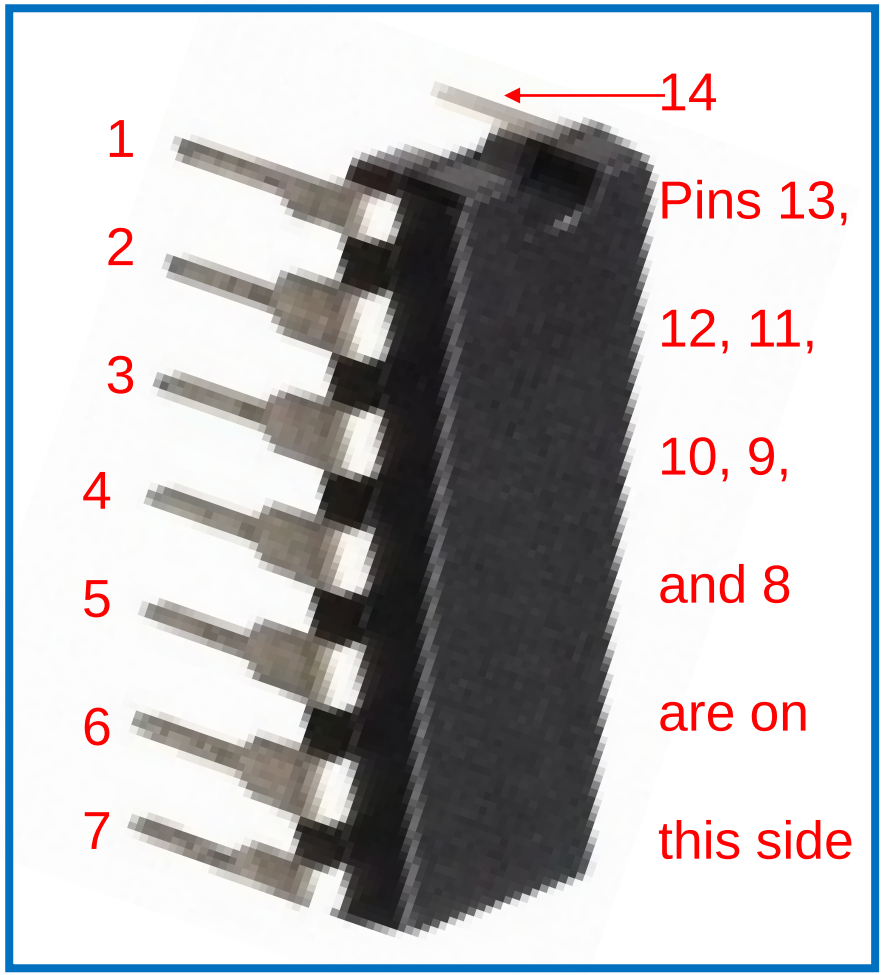
Integrated Circuits (ICs or chips) is made up of resistors, diodes and transistors fabricated on a single piece of semiconductor

74HCT00 Pin configuration



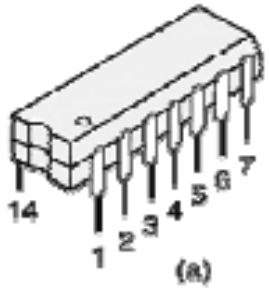
74HCT00 Pin configuration

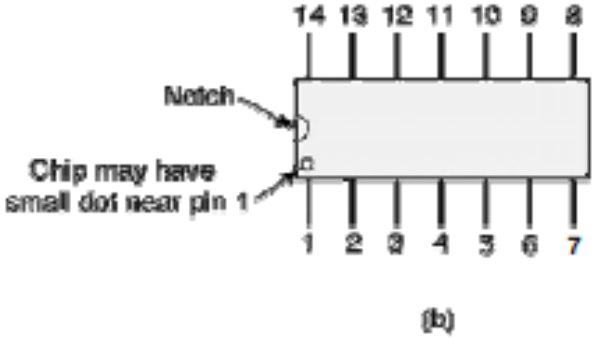




Basic Characteristics of Digital ICs

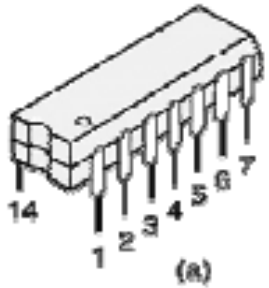
- Digital Integrated Circuits (ICs or chips): a collection of resistors, diodes and transistors fabricated on a single piece of semiconductor material
- The semiconductor is usually silicon (Si)

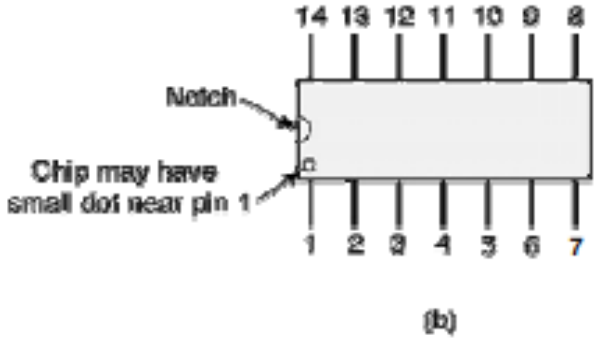


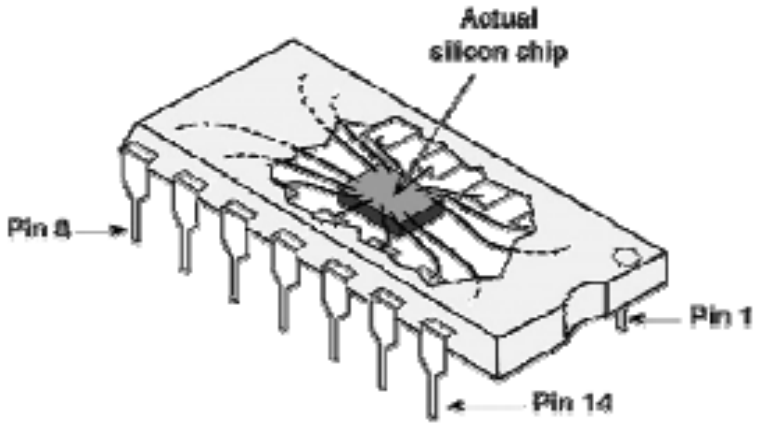


Basic Characteristics of Digital ICs

- Digital Integrated Circuits (ICs or chips): a collection of resistors, diodes and transistors fabricated on a single piece of semiconductor material
- The semiconductor is usually silicon (Si)
- Dual-in-line package (DIP) is a common type of packaging







2.2 Use of device datasheets

All the information we should need on the use of a particular integrated circuit should be available in the datasheet supplied by the manufacturer. **It is then essential that we refer to these datasheets when we construct a circuit.** Datasheets are available on the web; for example search for "74HCT00" and you will come across datasheets from different manufacturers for the device. Device properties between different manufacturers are typically very similar, and will provide you with all the electrical, timing and mechanical characteristics you need to use the IC.

2.3 Use of the design station and breadboard.

In these laboratories we will mostly use a commercial design station and breadboard to prototype your circuits. The functions and use of these will be explained to you at the start of the laboratory.

2.4 Implementing logic functions with a multiplexer (MUX)

A multiplexer is one of the special function integrated circuits that will be discussed in more detail later in the course. It has multiple inputs, a single output and a number of "input select lines" that will determine which one of the multiple input lines will be switched through to the output. It behaves like a rotary switch in that one of these inputs is steered through to the output depending upon the status of "input select" lines (also called control lines). This process is illustrated below for a 4:1 MUX. We can now hardwire a logic function on the MUX by connecting the input lines to the logic value that will be required as the output value Z for the given inputs A and B.

74HC00; 74HCT00

Quad 2-input NAND gate

Rev. 7 — 25 November 2015 Product data sheet

1. General description

The 74HC00; 74HCT00 is a quad 2-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC00: CMOS level
  - For 74HCT00: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC00D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT00D				
74HC00DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT00DB				
74HC00PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT00PW				
74HC00BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT00BQ				

4. Functional diagram

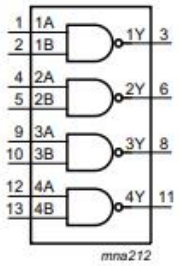


Fig 1. Logic symbol

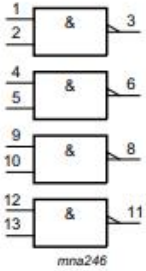


Fig 2. IEC logic symbol

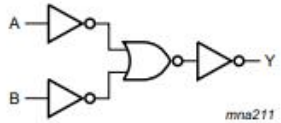


Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

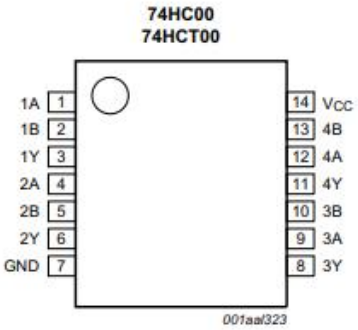
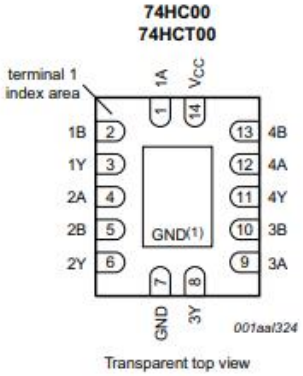


Fig 4. Pin configuration SO14 and (T)SSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN14

2.2 Use of device datasheets

All the information we should need on the use of a particular integrated circuit should be available in the datasheet supplied by the manufacturer. **It is then essential that we refer to these datasheets when we construct a circuit.** Datasheets are available on the web; for example search for "74HCT00" and you will come across datasheets from different manufacturers for the device. Device properties between different manufacturers are typically very similar, and will provide you with all the electrical, timing and mechanical characteristics you need to use the IC.

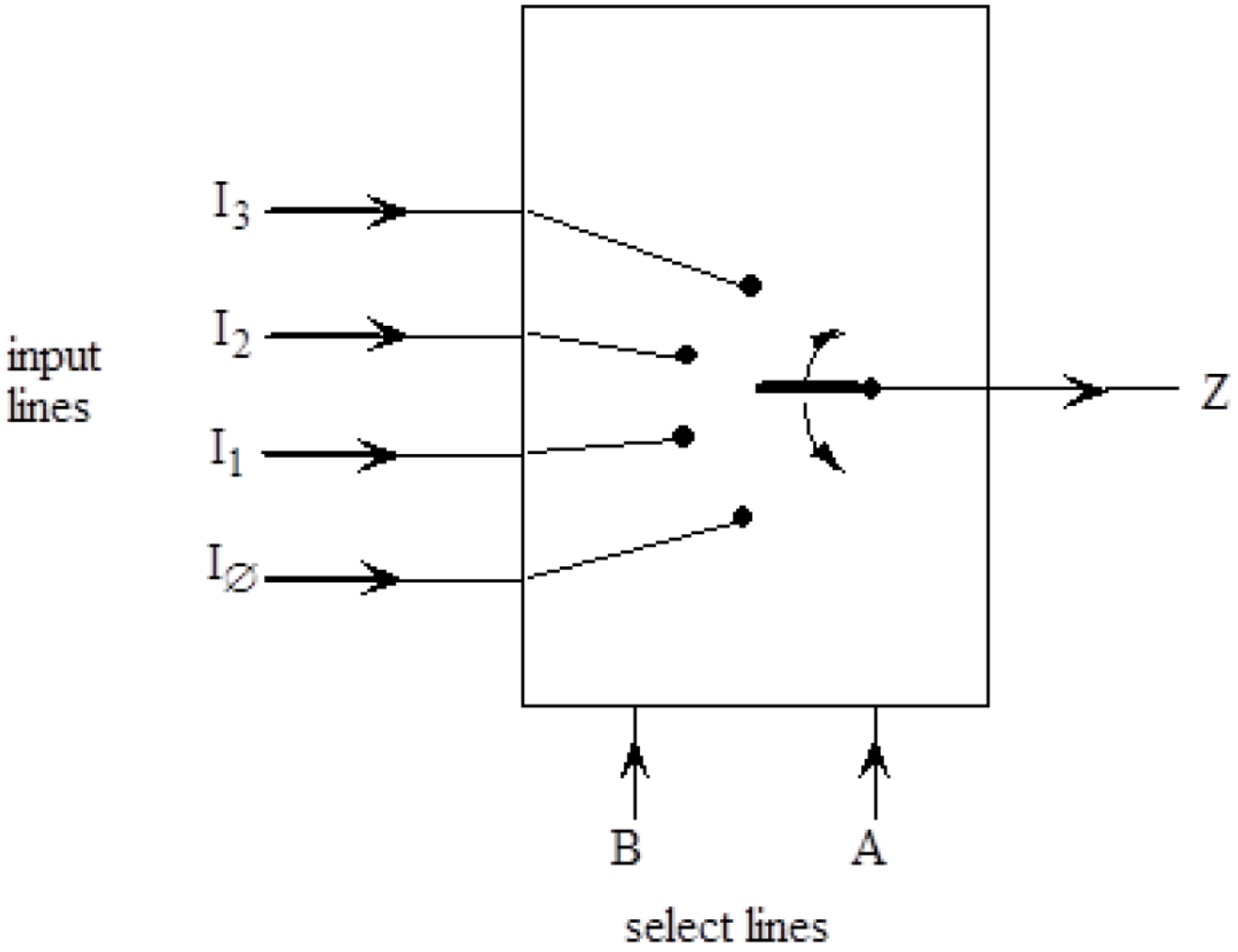
2.3 Use of the design station and breadboard.

In these laboratories we will mostly use a commercial design station and breadboard to prototype your circuits. The functions and use of these will be explained to you at the start of the laboratory.

2.4 Implementing logic functions with a multiplexer (MUX)

A multiplexer is one of the special function integrated circuits that will be discussed in more detail later in the course. It has multiple inputs, a single output and a number of "input select lines" that will determine which one of the multiple input lines will be switched through to the output. It behaves like a rotary switch in that one of these inputs is steered through to the output depending upon the status of "input select" lines (also called control lines). This process is illustrated below for a 4:1 MUX. We can now hardwire a logic function on the MUX by connecting the input lines to the logic value that will be required as the output value Z for the given inputs A and B.

Multiplexer (MUX)



3. Pre-lab Preparations

3.1 Reading

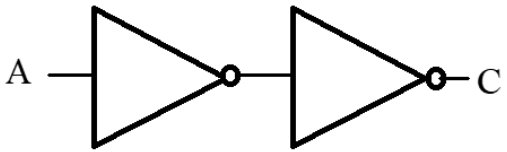
Review the Lecture slides on Logic Gates!

3.2 Complete the following work in your lab notebook before you attend the lab.

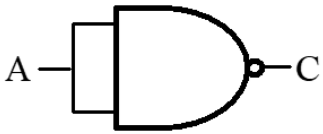
3.2.1 Draw up the truth tables for one of the four gates on each of the 74HCT00, 74HCT02 & 74HCT04 packages.

3.2.2 Use data sheets (available on the web) to sketch the pin-outs for each of the devices 74HCT00, 74HCT02 and 74HCT04. Note that (i) pin #1 is marked by a dot on the IC case, and the pins are numbered anticlockwise when viewed from above, (ii) pin #14, usually (but not always) reserved for the +5V power supply, and pin #7, usually common, are at opposite corners of the IC.

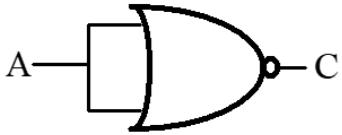
3.2.3 Establish truth tables relating the inputs A and B to the output C for the circuits below. Summarise the truth tables with algebraic expressions which reflect the relevant theorems of Boolean algebra.



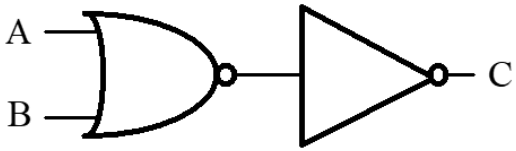
2/6 7404

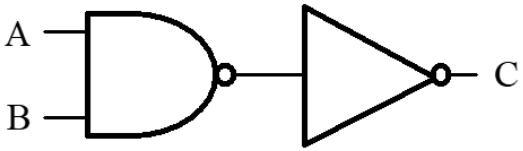


1/4 7400

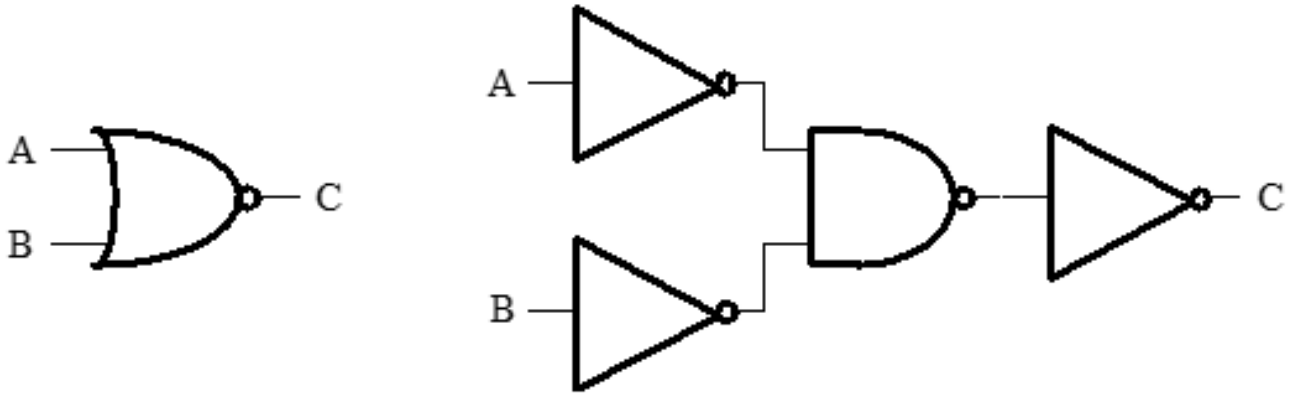


1/4 7402





3.2.4 Demonstrate one of De Morgan's two laws by establishing truth tables for the two circuits below. Write down algebraic expressions for the outputs C in both cases and show them to be equal by reference to their truth tables.



Week 9 Lecture 1b

- Lab 1 – Overview