Family Name:. . . . .   **Other Names:** . . . .

Student ID:. . . . .   **Signature** . . . .

ECEN 202: Final exam

2019, Dec 23

Instructions

- Time allowed: **120 minutes**
- Attempt **all** the questions. There are 45 marks in total.
- Write your answers in this exam paper and hand in all sheets.
- If you think some question is unclear, ask for clarification.
- You may use dictionaries.
- You may write notes and working on this paper, but make sure your answers are clear.

Questions   Marks

1. Microprocessors   [30]   [   ]

2. ADC and DAC   [15]   [   ]

                                                 TOTAL: [   ]

SPARE PAGE FOR EXTRA ANSWERS

Cross out rough working that you do not want marked.
Specify the question number for work that you do want marked.

Question 1. Microprocessors   [25 marks]

(a) **[1 mark]** What high-level computer architecture makes use of separate data and program memories?

(b) **[1 mark]** In a standard 8051, how many clock cycles result in one machine cycle?

(c) **[2 marks]** Given a 40 MHz crystal, find the time (in μs) required for one machine cycle

(d) **[2 marks]** Given a 12 MHz crystal, find the time (in μs) required for one machine cycle

(e) **[1 mark]** How many bits is Register A?

(f) **[1 mark]** What register holds the address of the next instruction to be executed?

(Question 1 continued)

(g) **[1 mark]** What is 0d16 in hexadecimal?

(h) **[1 mark]** On the 8051, what does the NOP instruction do?

(i) **[1 mark]** What instruction is used to add data to the stack?

(j) **[1 mark]** What instruction is used to remove data from the stack?

(k) **[1 mark]** What addressing mode is used by the following instruction? MOV A, R7

(Question 1 continued)

(l) **[1 mark]** Multiple choice (circle one of 1-4): On the 8051, when MOV A,B is called, which of the following occurs?

  1. The contents of B are moved to A, with B's contents being cleared after this operation
  2. The contents of a A are moved to B, with A's contents being cleared after this operation.
  3. The contents of B are moved to A, with B's contents being retained after this operation.
  4. The contents of a A are moved to B, with A's contents being retained after this operation.

(m) **[1 mark]** Multiple choice (circle one of 1-4): On the 8051, which of the following instructions is directly associated with a subroutine call?

  1. LJMP
  2. SJMP
  3. ACALL
  4. INC

(n) **[3 marks]** Briefly describe the role, function, and use of a **watchdog** timer

(o) **[2 marks]** Briefly describe the advantages of an interrupt-driven approach compared to a blocking/ polling approach.

(Question 1 continued)

(p) **[2 marks]** The initial contents of Register A are 0b11001100. What are the contents of Register A after the execution of an ORL instruction against A with an operand of 0b00110011?

[ ]

(q) **[2 marks]** The initial contents of Register A are 0b11111111. What are the contents of Register A after the execution of an ANL instruction against A with an operand of 0b00100000?

[ ]

(r) **[2 marks]** The A register has an initial value of 0b00000100

What are the register's contents after executing the following code?

```
RR A
RR A
ANL A, #10000011B
```

[ ]

(Question 1 continued)

(s) **[4 marks]** Timer mode information and details about the TMOD register are provided. Write code that sets Timer 0 to Mode 1 and Timer 1 to Mode 3. Assume that TMOD holds other values that must not be overwritten.

	Mode name
MODE 0	13-bit timer mode: 8 bits of THx and 5 bits of TLx
MODE 1	16-bit timer mode. TLx counts 0-255; on overflow, this adds 1 to THx
MODE 2	8-bit timer mode. TLx auto-reloads with THx value
MODE 3	"Split timer" mode: THx is one 8-bit timer, and TLx is another

TMOD.7 GATE	TMOD.6 C/T	TMOD.5 M1	TMOD.4 M0	TMOD.3 GATE	TMOD.2 C/T	TMOD.1 M1	TMOD.0 M0
When 1, timer only counts when TR1 bit is high and there is an external interrupt at INT0	When 0, Timer1 serves as XTAL-driven delay generator (timer); When 1, Timer1 counts external events	Timer 1 Mode bit 1 (see figure below for timer mode info.)	Timer 1 Mode bit 0 (see figure below for timer mode info.)	When 1, timer only counts when TR0 bit is high and there is an external interrupt at INT1	When 0, Timer0 serves as XTAL-driven delay generator (timer); When 1, Timer0 counts external events	Timer 0 Mode bit 1 (see figure below for timer mode info.)	Timer 0 Mode bit 0 (see figure below for timer mode info.)

Timer 0 Mode Select Bit

M10	M00	Operating mode
0	0	Mode 0: 8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0).
0	1	Mode 1: 16-bit Timer/Counter.
1	0	Mode 2: 8-bit auto-reload Timer/Counter (TL0) [2]
1	1	Mode 3: TL0 is an 8-bit Timer/Counter

TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits.

Question 2. ADC and DAC [15 marks]

(a) **[4 marks]** Sketch a circuit diagram of a four-bit binary-weighted Digital to Analogue Converter (DAC)

(b) **[2 marks]** Briefly describe the major advantage and disadvantage of a flash converter.

(c) **[1 mark]** A certain eight-bit successive-approximation converter has 2.55 V full scale. The conversion time for $V_A = 1$ V is 80 μs. What will be the conversion time for $V_A = 1.5$ V?

(Question 2 continued)

(d) **[8 marks]** For the following analogue to digital converters cases, calculate both the binary and decimal output code. Show your calculations.

i. **[4 marks]** An input voltage of 4.261 V into a 8-bit ADC with a 0 – 8 V input range.

ii. **[4 marks]** (ii) An input voltage of 2.295 V into a 10-bit ADC with a 0 – 4 V input range.

* * * * * * * * * * * * * *

SPARE PAGE FOR EXTRA ANSWERS

Cross out rough working that you do not want marked.
Specify the question number for work that you do want marked.