Practical embodiment of an A to D.

• Compare the incoming voltage to certain, set reference levels

• Set the binary output state according to this comparison.

Use a very handy electronic device called a comparator

The Comparator.

•Based on an operational amplifier

•Forms a neat interface between the analog and digital worlds

•It takes an analog signal at its input and compares it to a reference analog signal.

•Depending on the input, the output of the comparator is either LO or HI (binary output).

| Input signal	Output signal
Vin < Vref	LO
Vin > Vref	HI

Can be described as a single bit analog to digital converter !

(a)   (b)
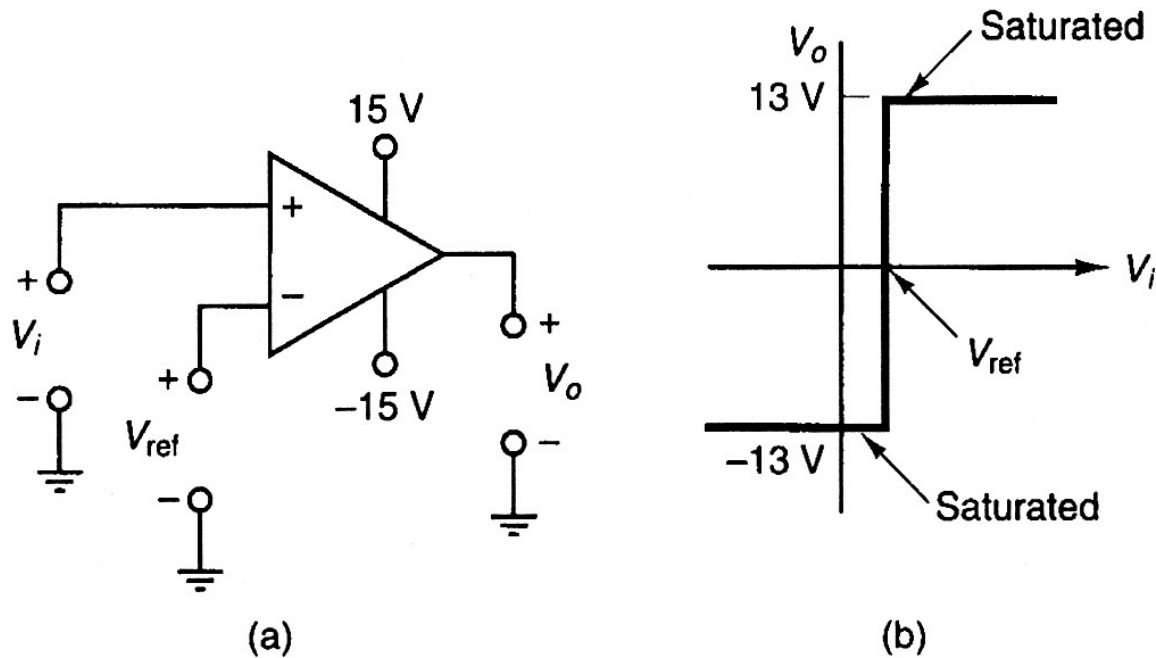
Voltage divider

- When a voltage is applied to a series combination of resistances, a fraction of voltage appears across each of the resistance.

- A series circuit acts as a voltage divider. The voltage divider is an important application of series circuits.

- A circuit consisting of a series string of resistors connected to a voltage source acts as a voltage divider.

How to calculate voltage in voltage divider?
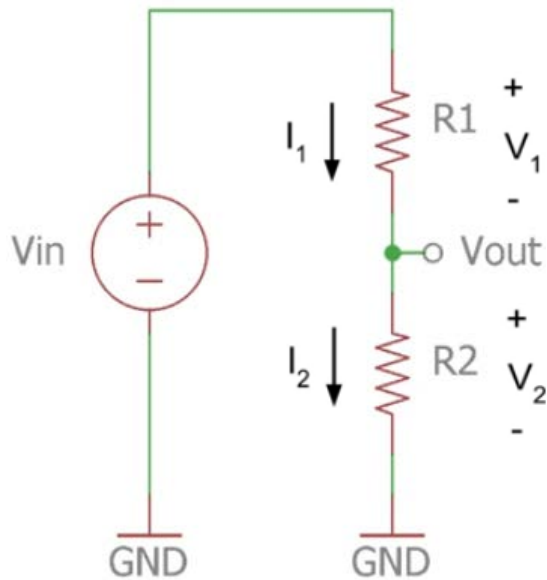
$$V_{out} = V_2$$

$$V_{out} = I_2 \times R_2$$

$$I_2 = I_1 = I$$

$$V_{out} = I \times R_2$$

$$I = \frac{V_{out}}{R_2}$$
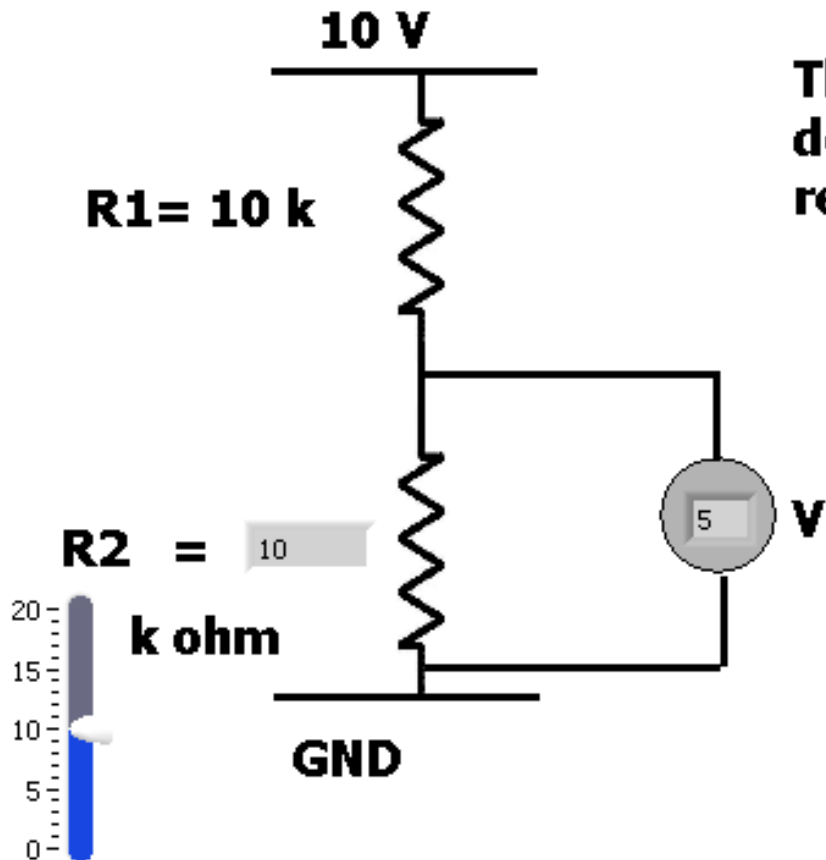
$$V_{in} = I \times R$$

$$R = R_1 + R_2$$

$$V_i = I \times (R_1 + R_2)$$

$$I = \frac{V_{in}}{(R_1 + R_2)}$$

$$\frac{V_{out}}{R_2} = \frac{V_{in}}{(R_1 + R_2)}$$

$$V_{out} = V_2 \times \frac{R_2}{R_1 + R_2}$$

The resistor chain - A simple method to create a series of reference voltages.

10 V

R1= 10 k

R2 = 10

k ohm

GND

The voltage over the resistors devide in the ratio of their respective resistances

5 **V** = **10 V * R2/(R1+R2)**

$$= 10\ V *\ \frac{10}{(\ 10\ + 10\ )}\ k\ ohm$$

20
15
10
5
0

The operation of many types of A/D are based on or use the comparator.

We will look at three types:

(1) The flash converter

(2) The ramp/staircase converter

(3) The successive approximation (SAC) converter

FLASH Converter

- Compare the incoming analogue voltage to reference voltage levels and decide which reference levels does best represent it.

- Convert this reference level to a binary code, using a predetermined number of bits.

- Convert the binary code to a decimal number to make it easy for the operator to interact.

Operation of a 3-bit parallel (flash) A/D

Assume an input range of 0 – 7 V

Each "step" is 1 V as created by resistor chain voltage divider
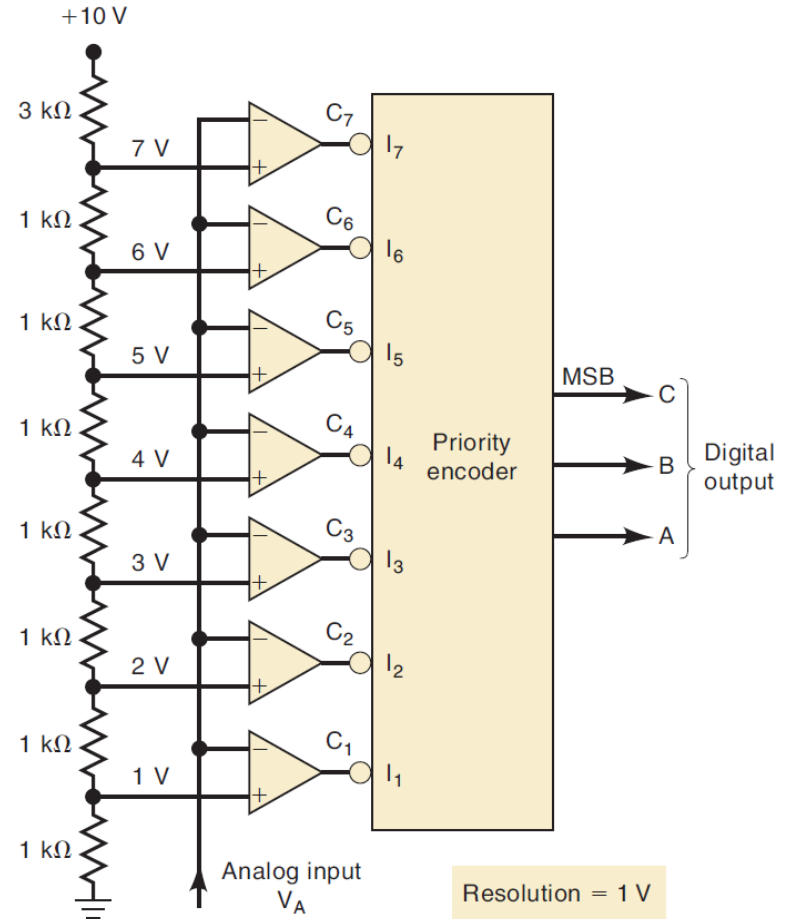
To represent 8 steps we will need 3 bits – 8 possible OP states.

To determine which is the highest active level we need 7 comparators

Thus need $2^n - 1$ comparators

Need 2^n resistors

Need priority encoder to code from 7 IPs to 3-bit code

Analog in	Comparator outputs							Digital outputs		
V_A	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C	B	A
0–1 V	1	1	1	1	1	1	1	0	0	0
1–2 V	0	1	1	1	1	1	1	0	0	1
2–3 V	0	0	1	1	1	1	1	0	1	0
3–4 V	0	0	0	1	1	1	1	0	1	1
4–5 V	0	0	0	0	1	1	1	1	0	0
5–6 V	0	0	0	0	0	1	1	1	0	1
6–7 V	0	0	0	0	0	0	1	1	1	0
> 7 V	0	0	0	0	0	0	0	1	1	1

The parallel or flash A/D converter

•Very fast converter

•Compares the analogue voltage to all reference levels simultaneously. No clock signal is used, so the conversion is continuous.

•We would need a comparator for every step (reference levels – 1). Thus to output n bits we would need 2^n-1 comparators. 10 bit flash ADC requires 1023 comparators!

•Use resistor based voltage divider

•Use decoder to change comparator output into binary number

•Very expensive due to high number of comparators

•Used only in high end (expensive) A/D's where speed is important

Feedback ADCs

- The ADC uses a DAC and a comparator.
- A guess is applied to the DAC and the resulting output is compared with the input.
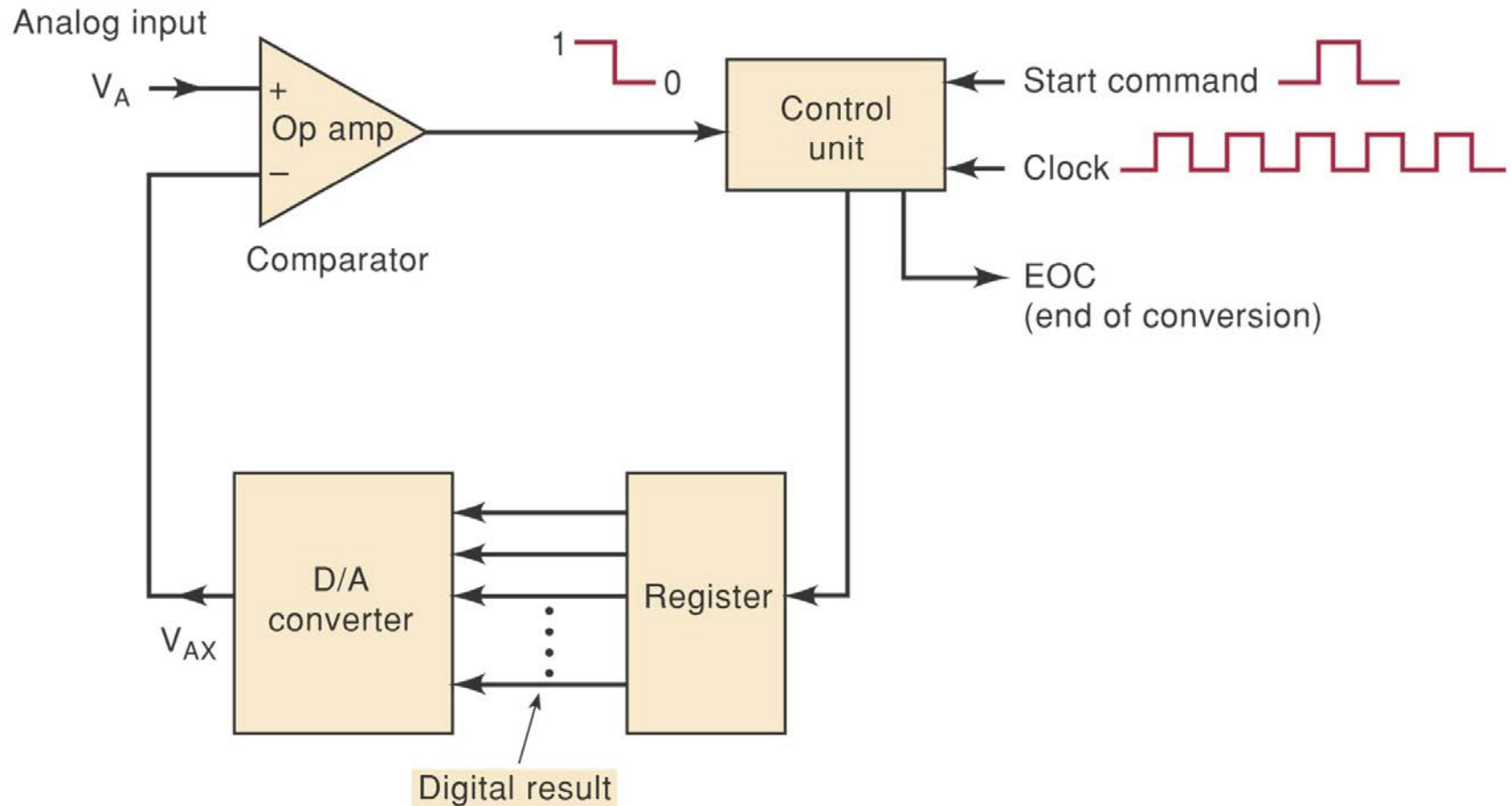
The ramp/staircase/counter ADC

• Uses a binary up counter

• Feeds counter into digital to analog converter

• DAC generates an analog voltage representing the binary count of the counter

• This increasing analog voltage is compared by comparator to the analog voltage to be measured (V_{in}) and the comparator will change state when $V_{DAC} > V_{in}$

• This comparator transition will stop the counter and also signal "End Of Conversion" The counter value representing the binary conversion of the analog voltage.

The ramp/staircase/counter ADC

(a)

(b)
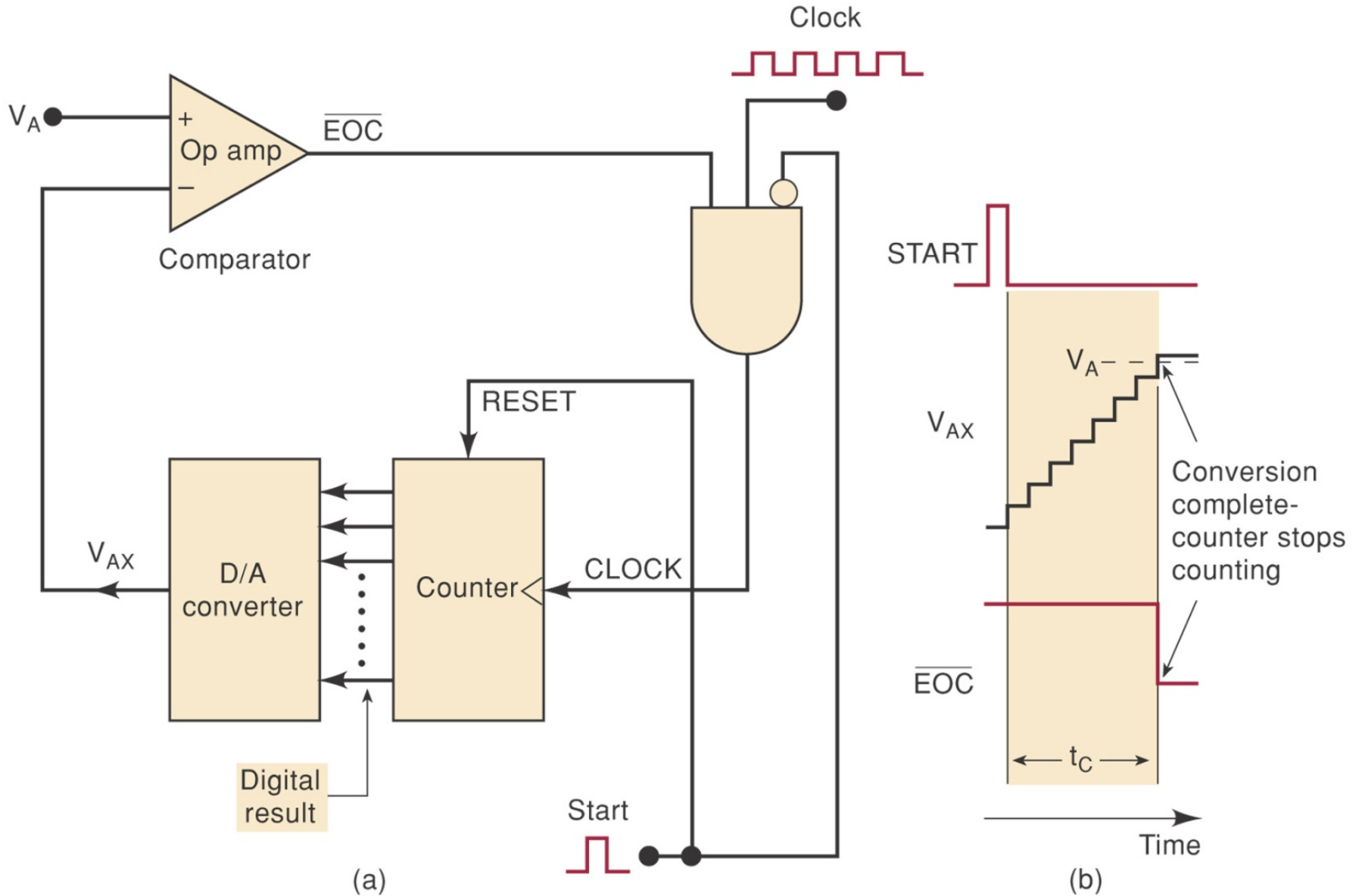
Problem:

Assume the following values for the digital-ramp ADC, clock frequency = 1 MHz; V_T = 0.1 mV; DAC has F.S. output = 10.23 V and a 10-bit input. Determine the following values.

(a) The digital equivalent obtained for V_A = 3.728 V

(b) The conversion time

(c) The resolution of this converter

Solution:

(a) The DAC has a 10-bit input and a 10.23-V $_{F.S.}$ output. Thus, the number of total possible steps is 2^{10} - 1 = 1023, and so the step size is 10.23 V/ 1023 = 10 mV

This means that V_{AX} increases in steps of 10 mV as the counter counts up from 0.

Because V_A = 3.278 V and V_T = 0.1 mV, V_{AX} must reach 3.7281 V for more before the comparator switches LOW. This will require

3.7281 V/10 mV = 372.81 = 373 steps

At the end of the conversion, then, the counter will hold the binary equivalent of 373, which is 0101110101. This is the desired digital equivalent of V_A = 3.728 V, as produced by this ADC.

Solution:

(b) 373 steps were required to complete the conversion. Therefore, 373 clock pulses occurred at the rate of one per microsecond. This gives a total conversion time of 373 μs

(c) The resolution of this converter is equal to the step size of the DAC, which is 10 mV. Expressed as a percentage, it is 1/1023 * 100 ≈ 0.1,.
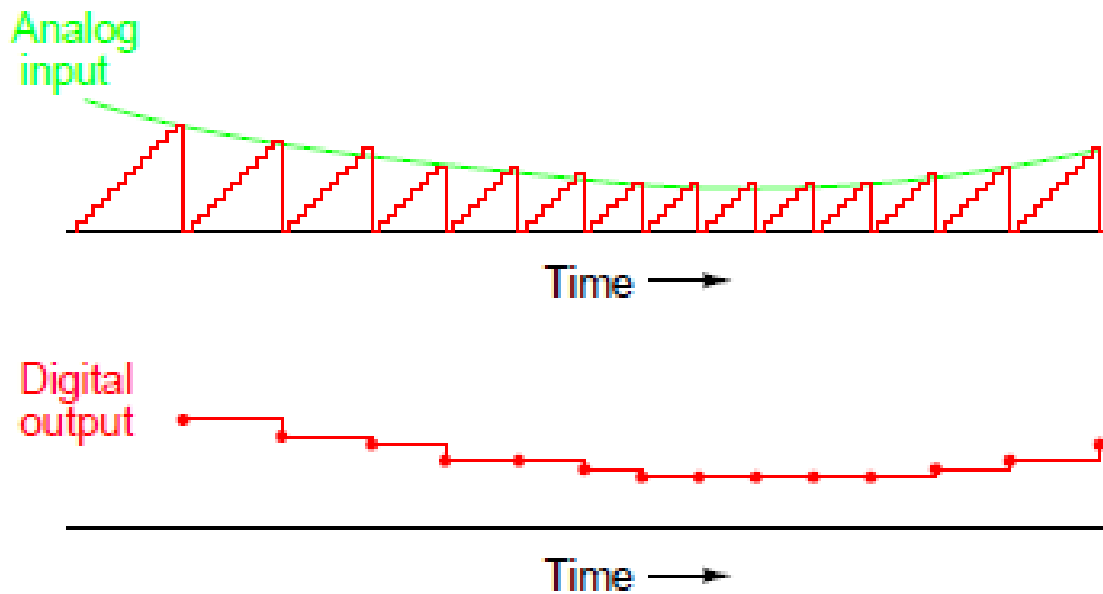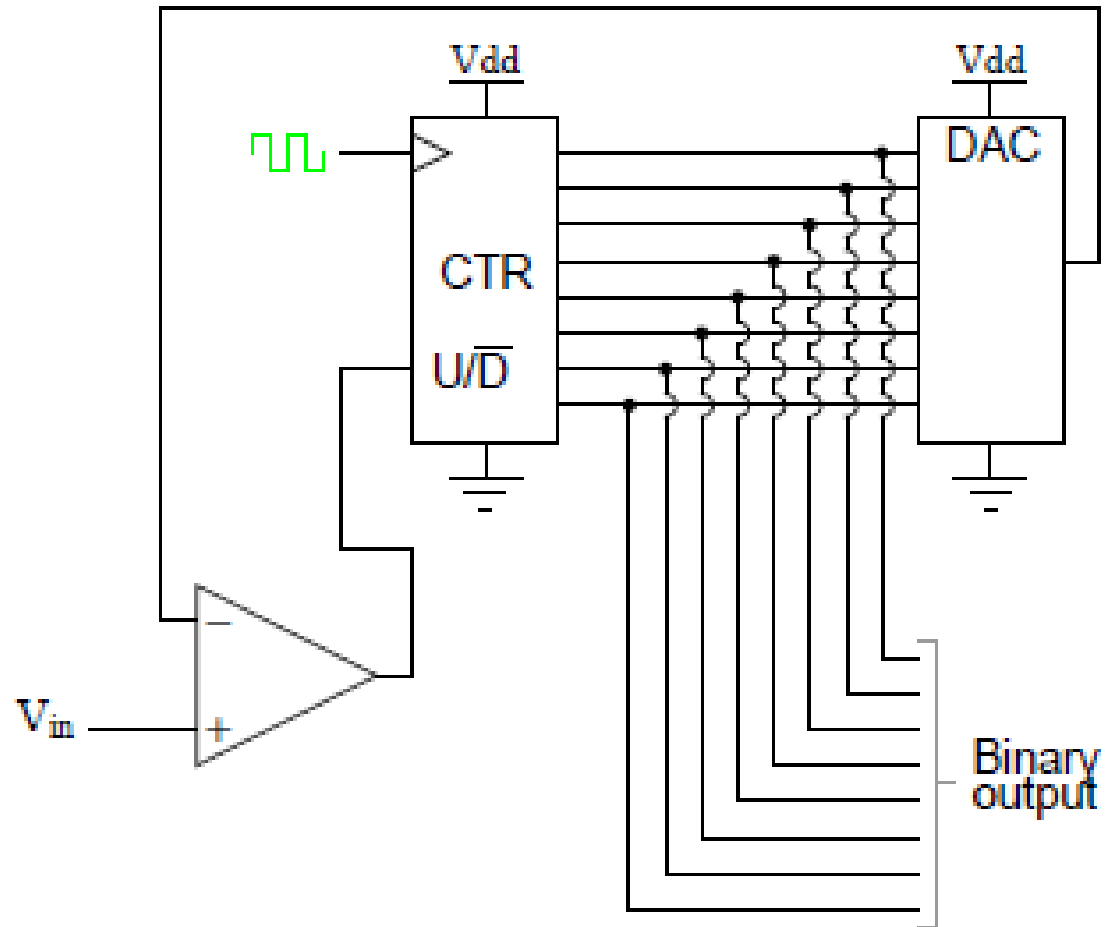
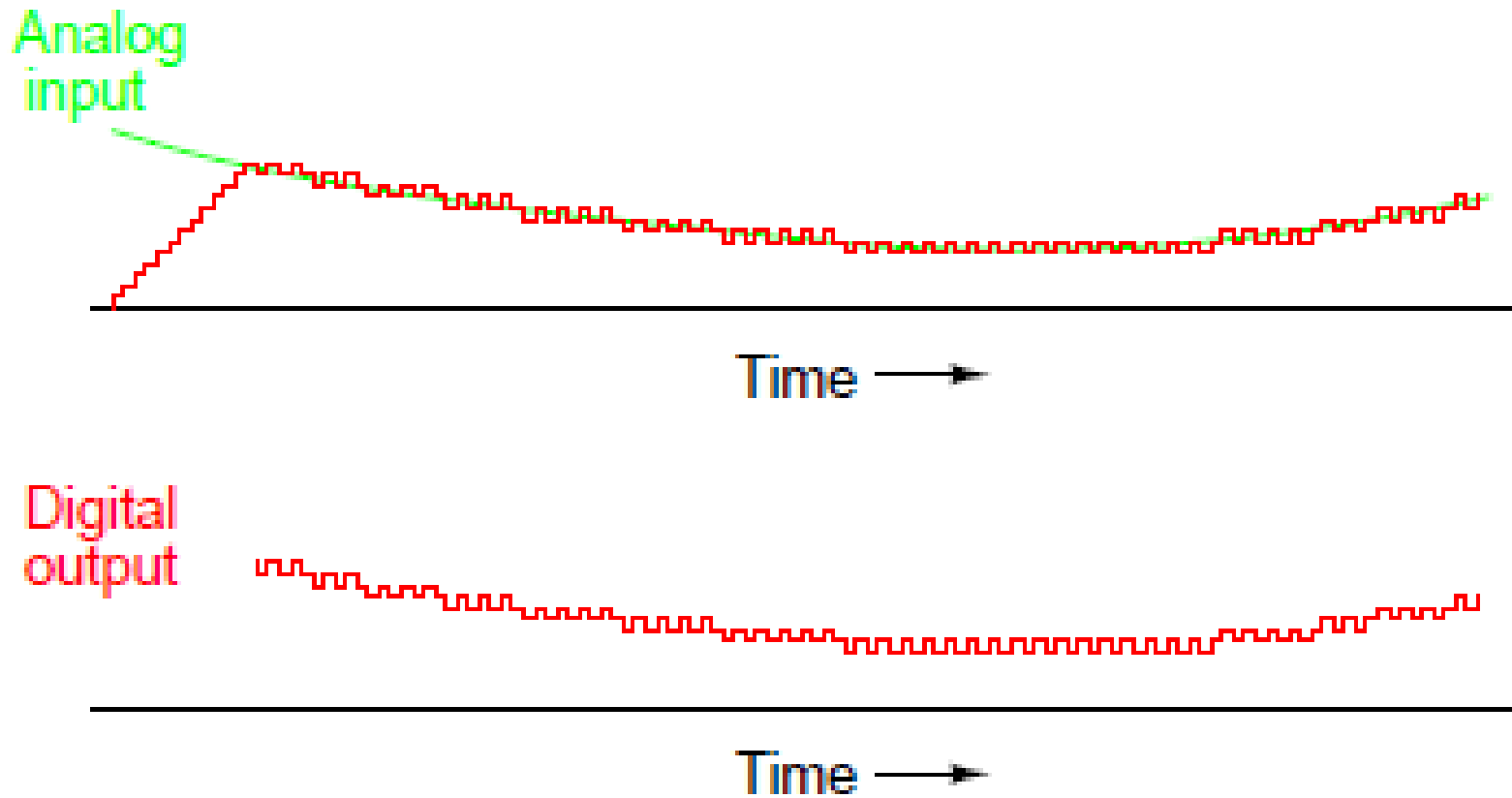Operation simple and easy to construct but:

Time to perform a conversion is not constant – depends on the magnitude of V_{in} – large voltage will take more clock cycles to convert.

Start counter at zero every time – makes it a relatively slow conversion process.

# The tracking ADC is an improvement on the staircase ADC

The tracking ADC

The successive approximation A/D

- One off the most popular types of ADC's

- Binary Search algorithm

- Relatively fast but affordable

- Has a fixed conversion time.

- Uses only one comparator but generates different reference signals for this comparator

- Uses a digital to analog converter (!) to generate a reference signal.

- Digital code is generated by a successive approximation register.

- Operation takes place based on an internal clock cycle

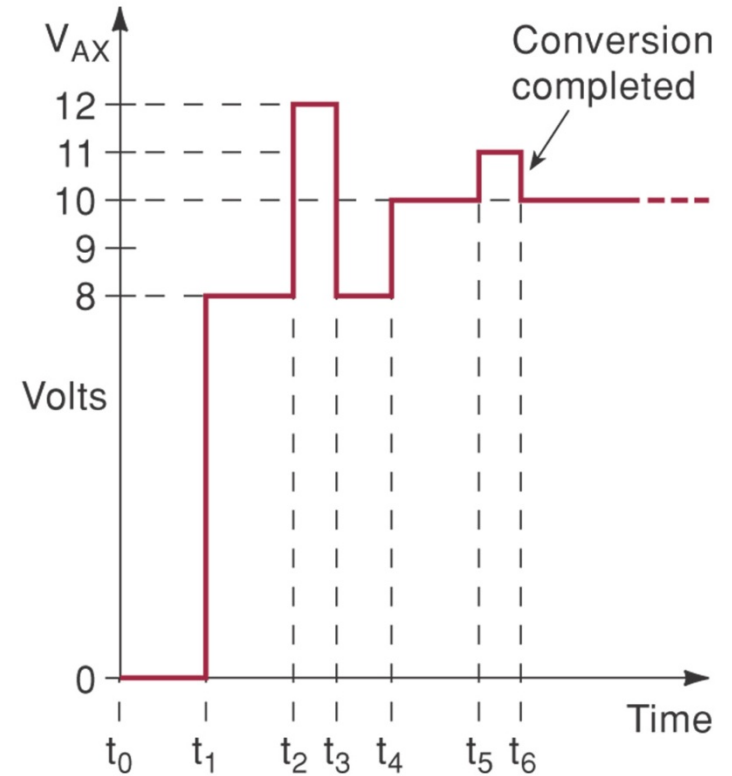Successive-approximation ADC: (a) simplified block diagram; (b) flowchart of operation.
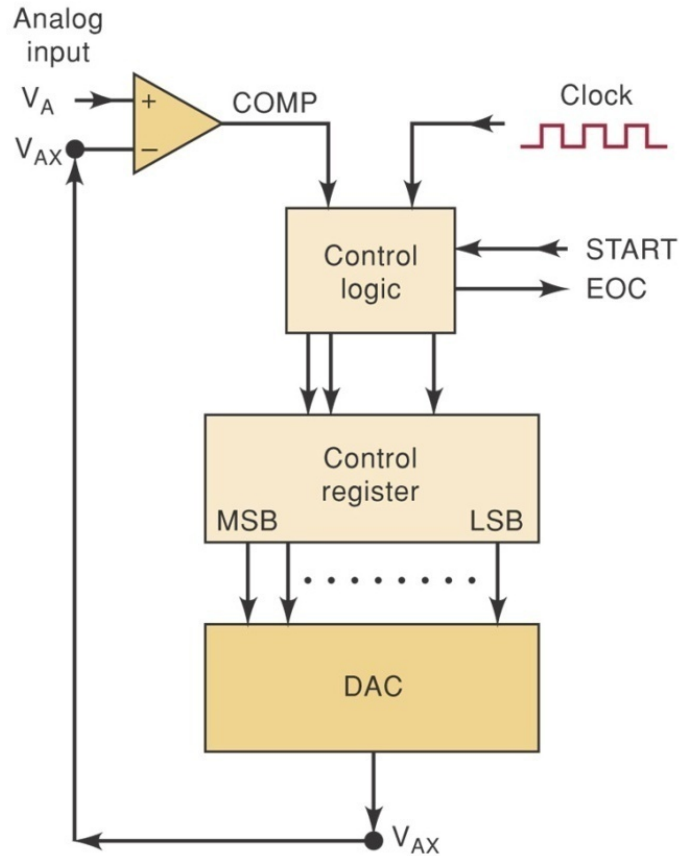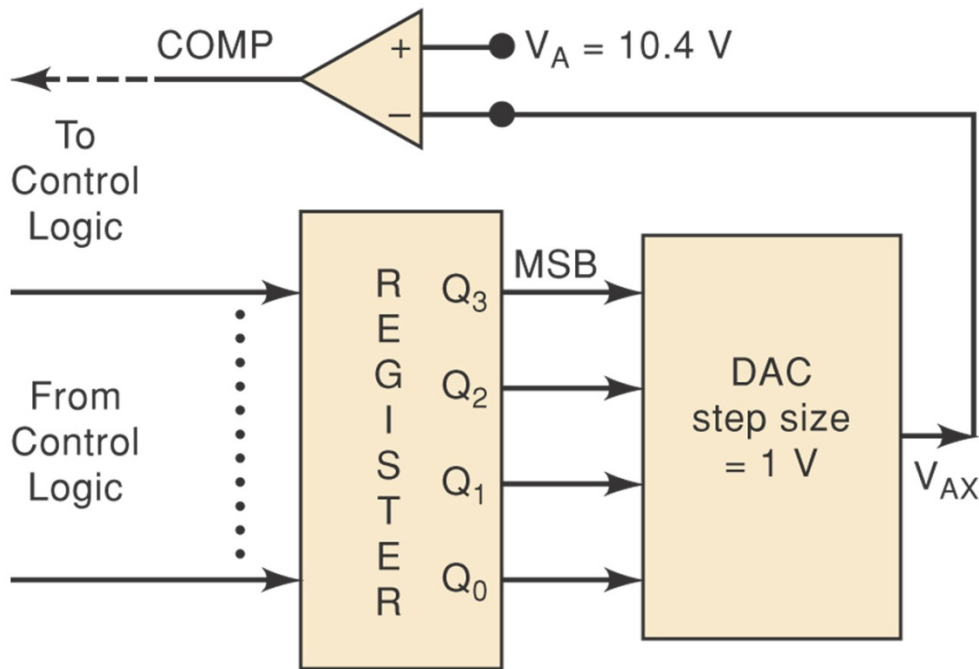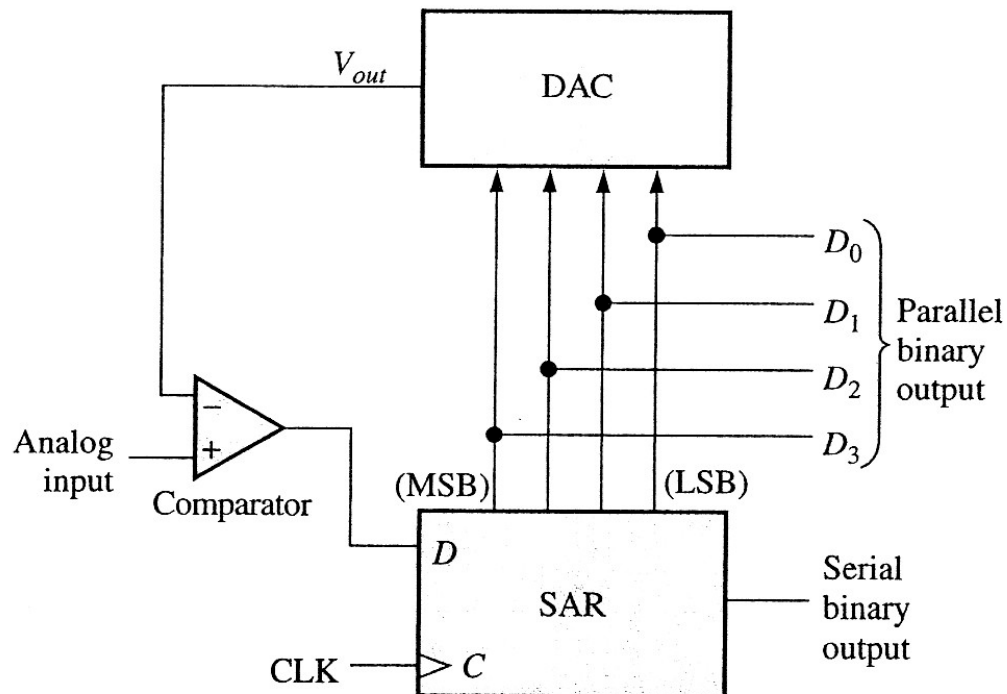

(a)
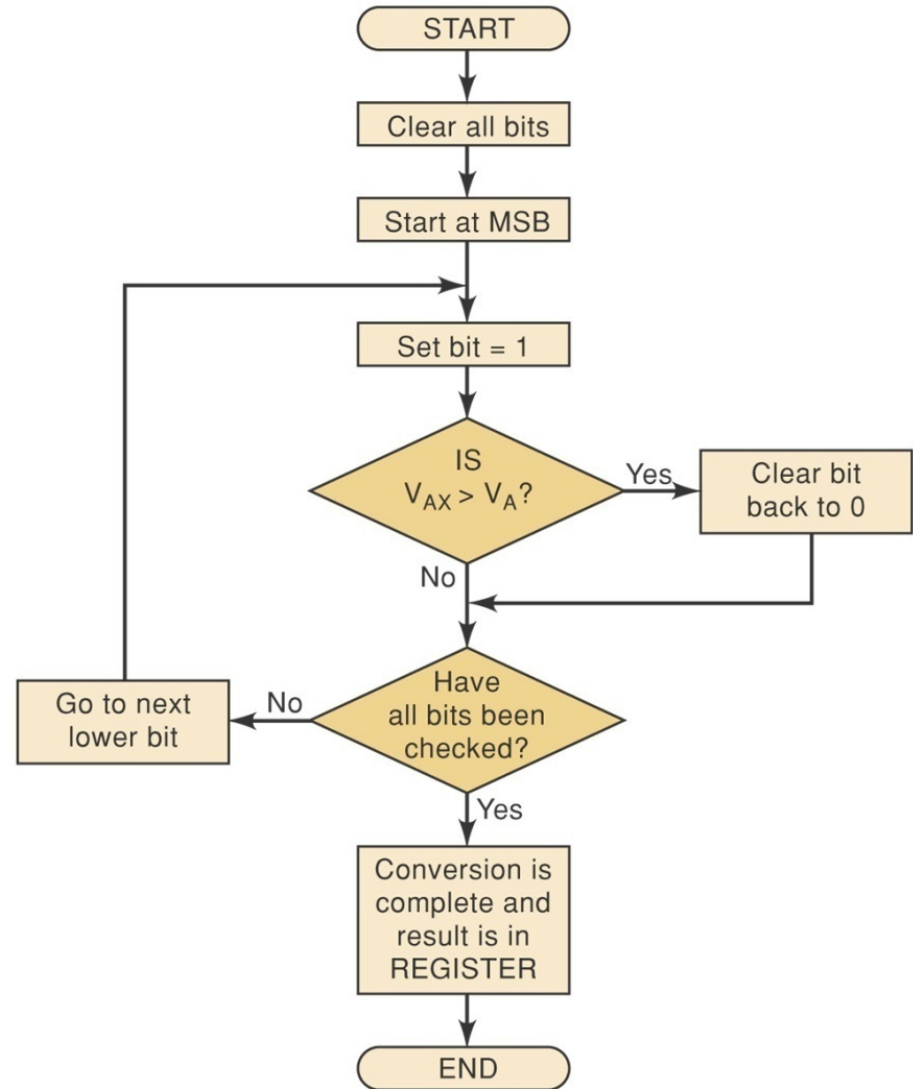
(b)

Illustration of four-bit SAC operation using a DAC step size of 1 V and V_A = 10.4 V.

Detailed Operation of a 4-bit successive approximation A/D

- Assume an A/D with a full scale input of 16 V

- Feed an analog input signal of 5.1 V into the A/D

- Represent the signal with a 4-bit binary code.

• On the first approximation cycle the MSB (the 2^3 bit) in the successive approximation register (SAR) goes HI and the binary code 1000 is put out to the digital to analog converter. This code will generate an analog output of 8 V from the DAC and this 8 V (half of full scale input) is now put out to the reference input of the comparator.

• The comparator compares the analog input signal (taken to be 5.1 V in this case) to this reference and the output state of the comparator is determined by this comparison.

• If the analog input voltage is lower than the reference (as it is in this case) the output of the comparator will be low and the MSB in the SAR will reset to a zero.

Comparing the MSB

(a) MSB trial

(b) 2^2-bit trial

(c) 2^1-bit trial

(d) LSB trial (conversion complete)
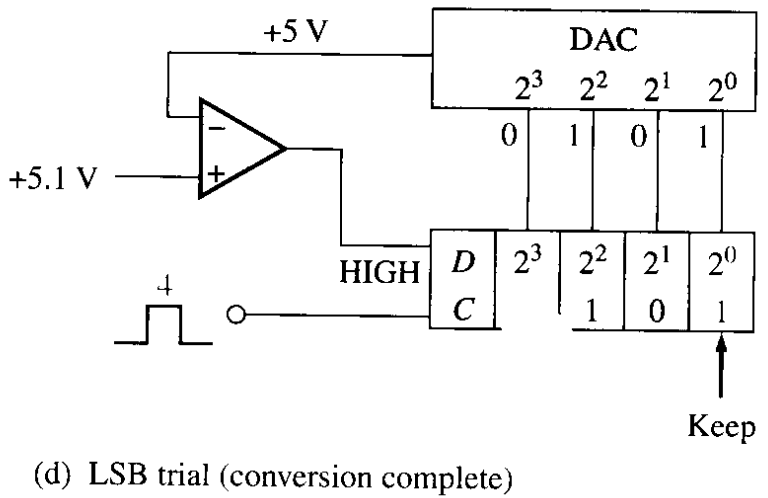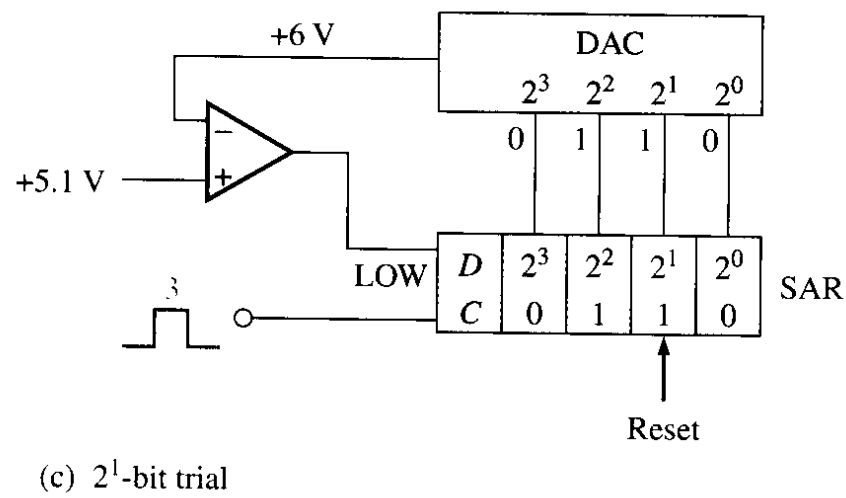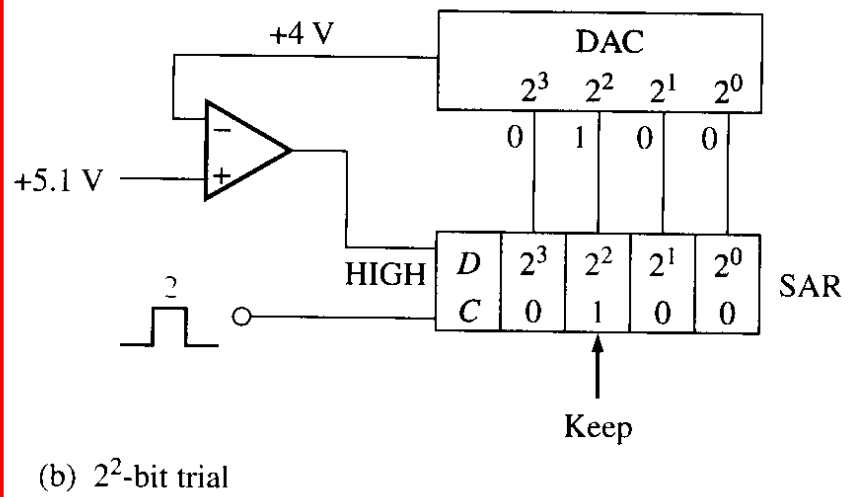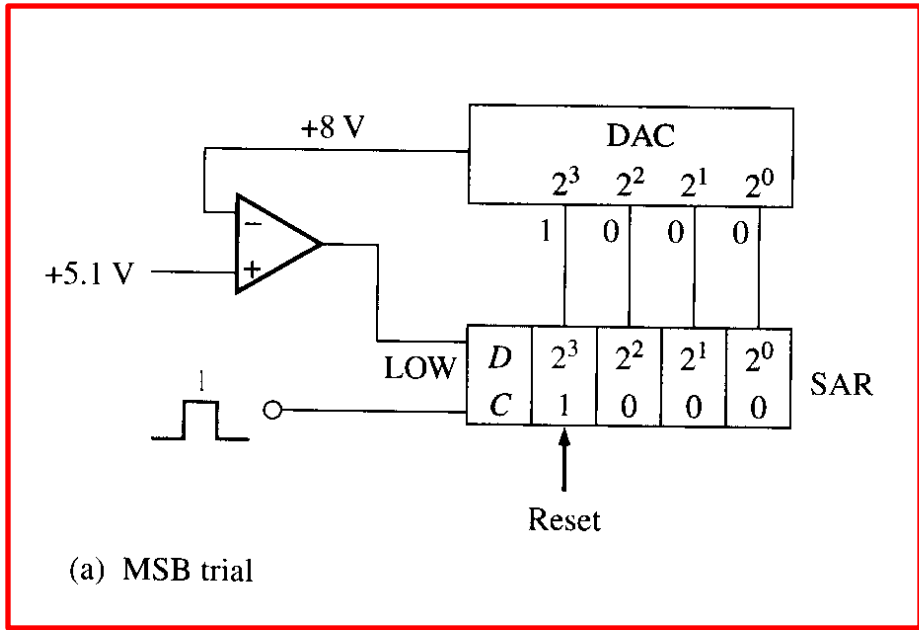
Comparing the second MSB

- The second MSB now goes HI and the code 0100 is put out to the DAC. This will produce an output of 4V from the DAC which now becomes the new reference signal of the comparator.

- The analog input signal is again compared to the reference and in this case it exceeds the reference.

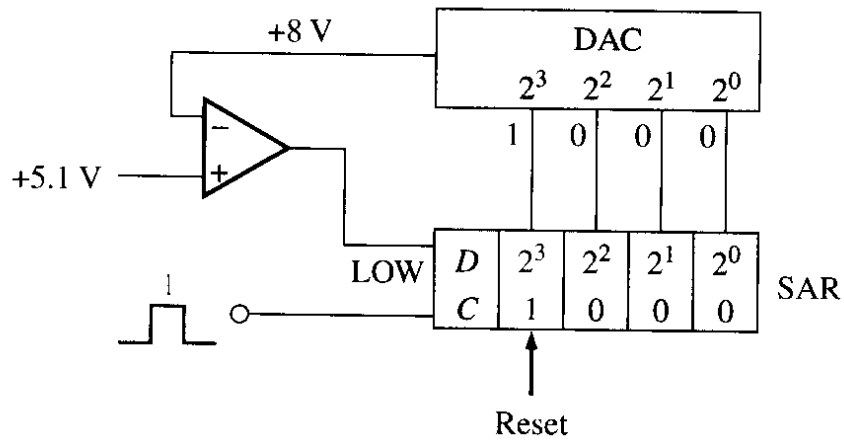- The output of the comparator will thus go HI and the value of "1" for the 2^2 bit is fixed in the SAR.

(a) MSB trial

+8 V

DAC

2^3	2^2	2^1	2^0
1	0	0	0

+5.1 V

LOW

D C	2^3	2^2	2^1	2^0	SAR
	1	0	0	0	

1

Reset

(a) MSB trial

(b) 2^2-bit trial

+4 V

DAC

2^3	2^2	2^1	2^0
0	1	0	0

+5.1 V

HIGH

D C	2^3	2^2	2^1	2^0	SAR
	0	1	0	0	

2

Keep

(b) 2^2-bit trial

(c) 2^1-bit trial

+6 V

DAC

2^3	2^2	2^1	2^0
0	1	1	0

+5.1 V

LOW

D C	2^3	2^2	2^1	2^0	SAR
	0	1	1	0	

3

Reset

(c) 2^1-bit trial

(d) LSB trial (conversion complete)

+5 V

DAC

2^3	2^2	2^1	2^0
0	1	0	1

+5.1 V

HIGH

D C	2^3	2^2	2^1	2^0
		1	0	1

4

Keep
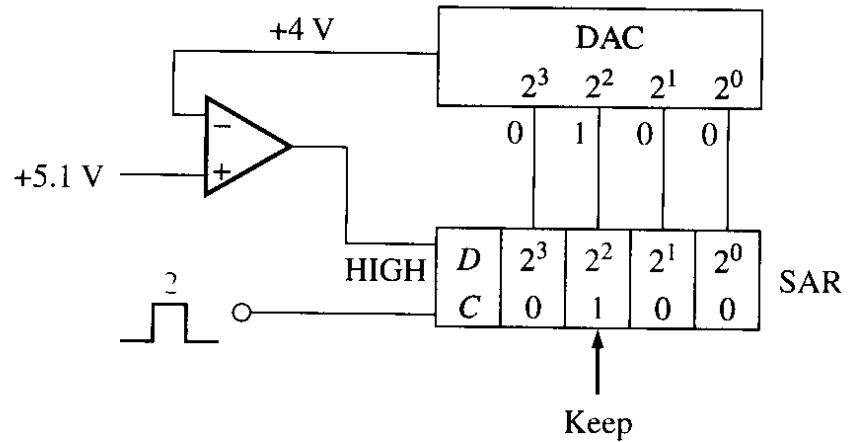
(d) LSB trial (conversion complete)
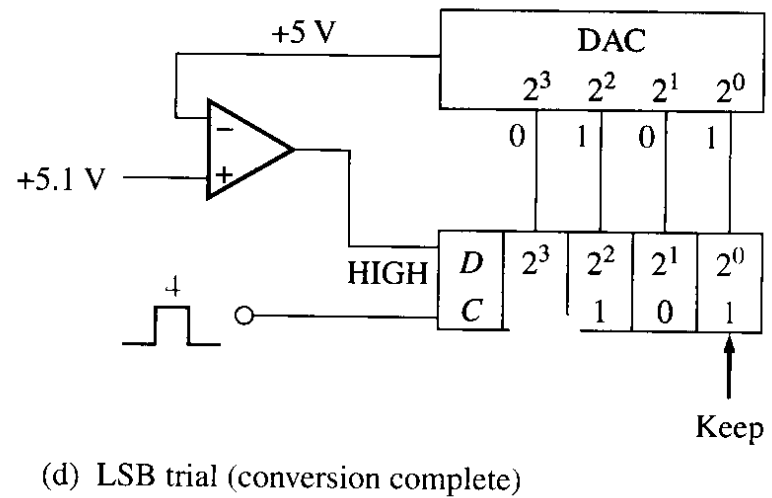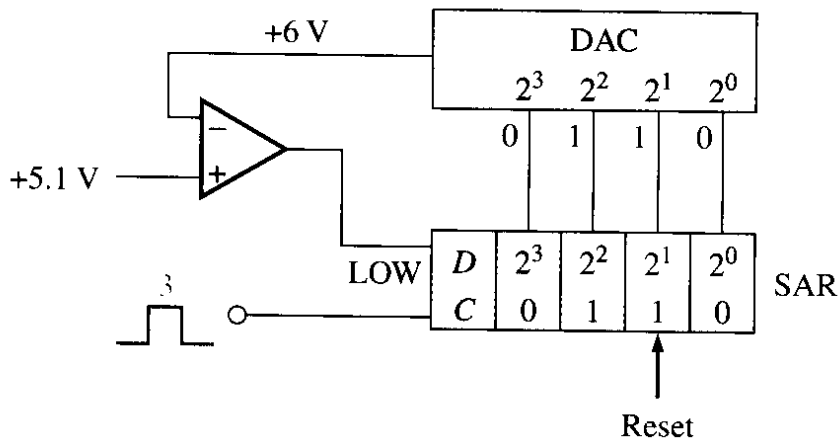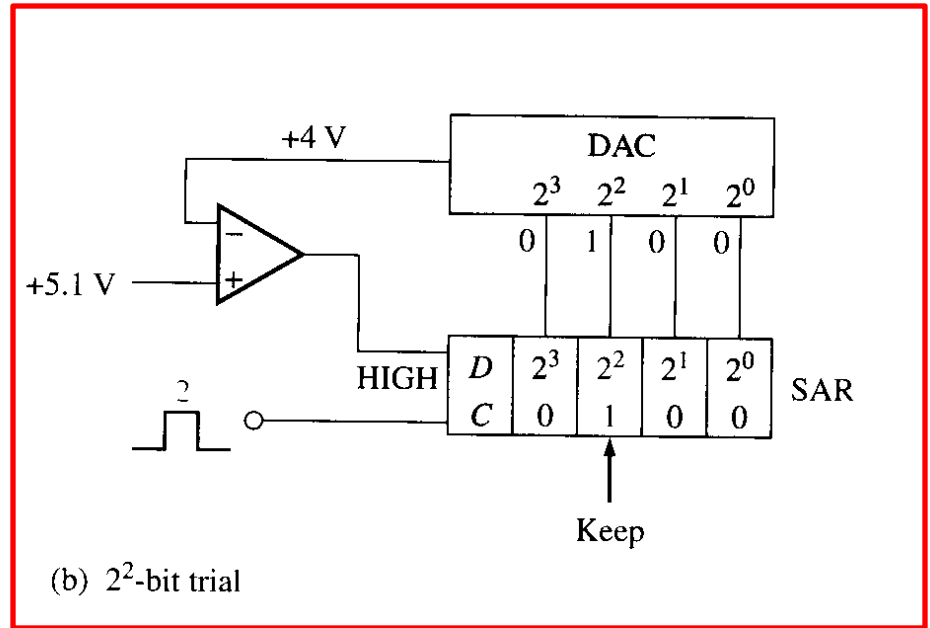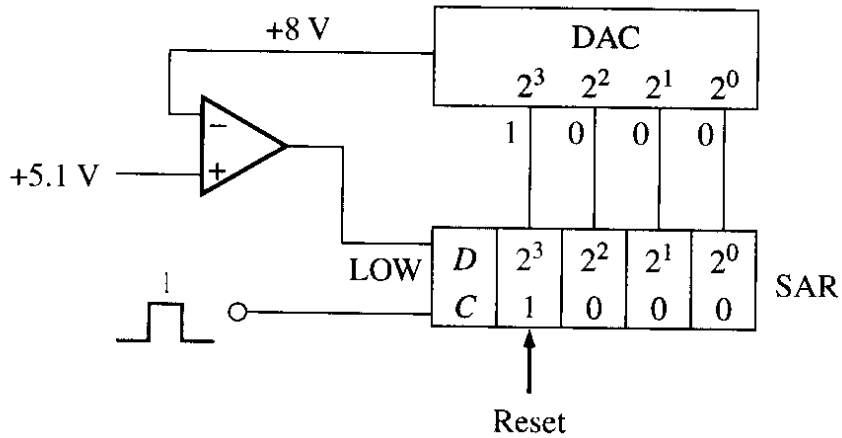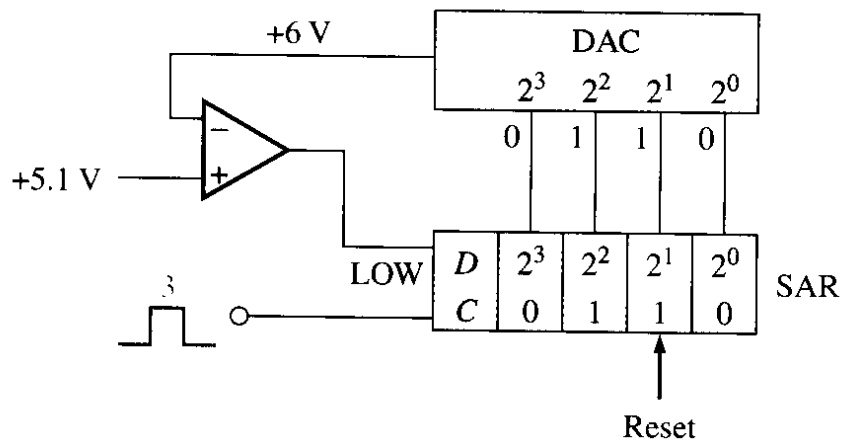
Comparing the third MSB

- The third MSB (the 2^1 bit) now goes HI and the code 0110 is put out to the DAC. (Remember the 2^2 bit is now fixed HI). This will produce a 6 volt output which is the new reference signal.

- The input signal is now lower than the reference and the output from the comparator will be LO. This will reset the 2^1 bit to zero again.
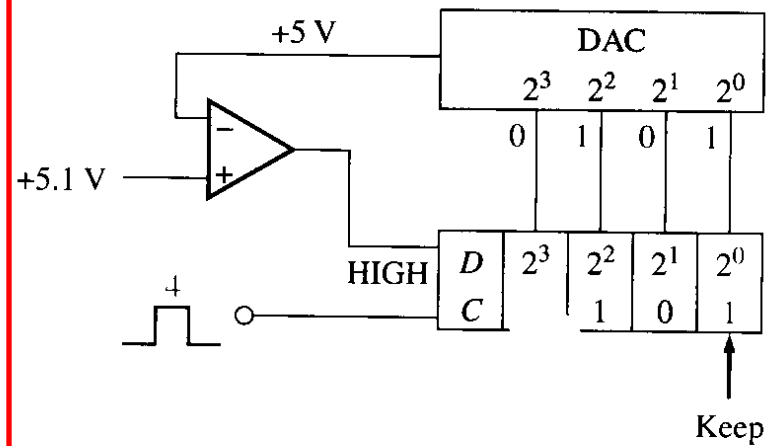
(a) DAC

+8 V

2^3 2^2 2^1 2^0
1   0   0   0

+5.1 V

LOW

D
C

SAR

2^3	2^2	2^1	2^0
1	0	0	0

1

Reset

(a) MSB trial

(b) DAC

+4 V

2^3 2^2 2^1 2^0
0   1   0   0

+5.1 V

HIGH

D
C

SAR

2^3	2^2	2^1	2^0
0	1	0	0

2

Keep

(b) 2^2-bit trial

(c) DAC

+6 V

2^3 2^2 2^1 2^0
0   1   1   0

+5.1 V

LOW

D
C

SAR

2^3	2^2	2^1	2^0
0	1	1	0

3

Reset

(c) 2^1-bit trial

(d) DAC

+5 V

2^3 2^2 2^1 2^0
0   1   0   1

+5.1 V

HIGH

D
C

2^3	2^2	2^1	2^0
	1	0	1

4

Keep
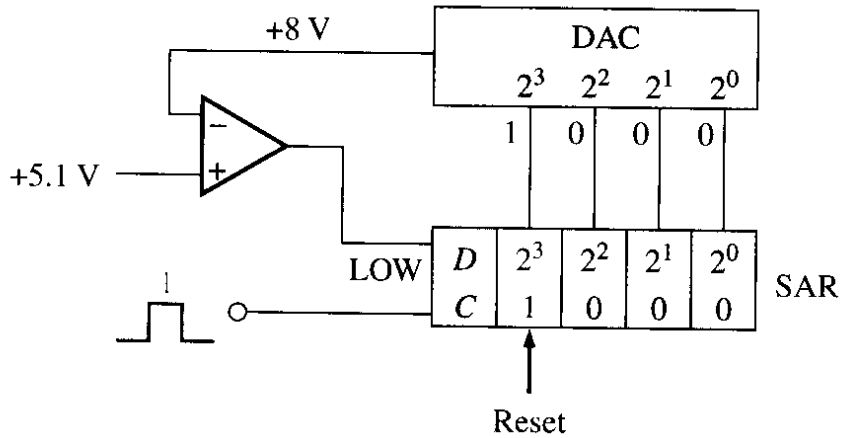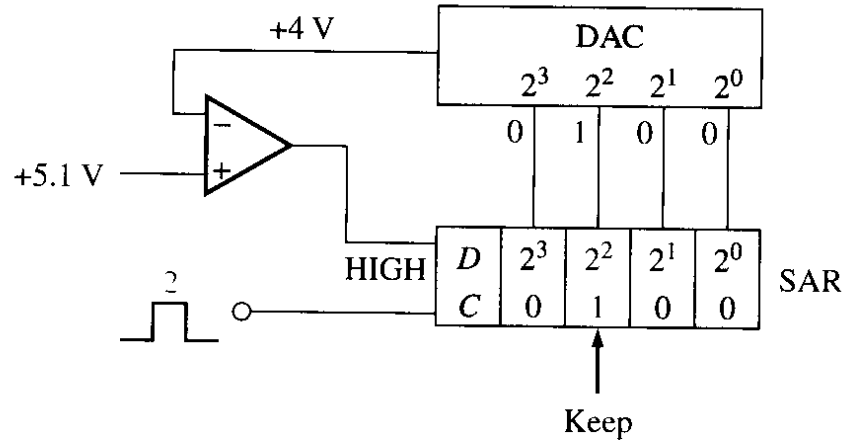
(d) LSB trial (conversion complete)

Comparing the LSB

* On the fourth comparison cycle the LSB (2^0 bit) will go HI and the code 0101 put out to the DAC. A reference voltage of 5 V will thus be put on the comparator.

* The input analog voltage is now higher than the reference voltage and the output of the comparator will go HI. This will fix the value of the LSB as "1"in the SAR.

* The conversion process is now complete and the binary number stored in the SAR (0101) can now be read by a microprocessor as representative of the 5.1 V analog input.
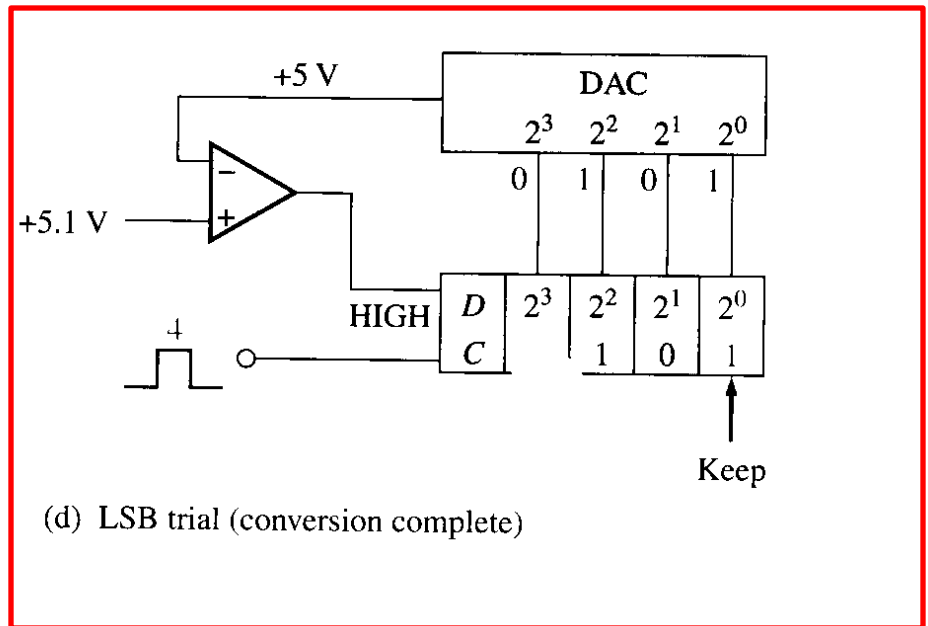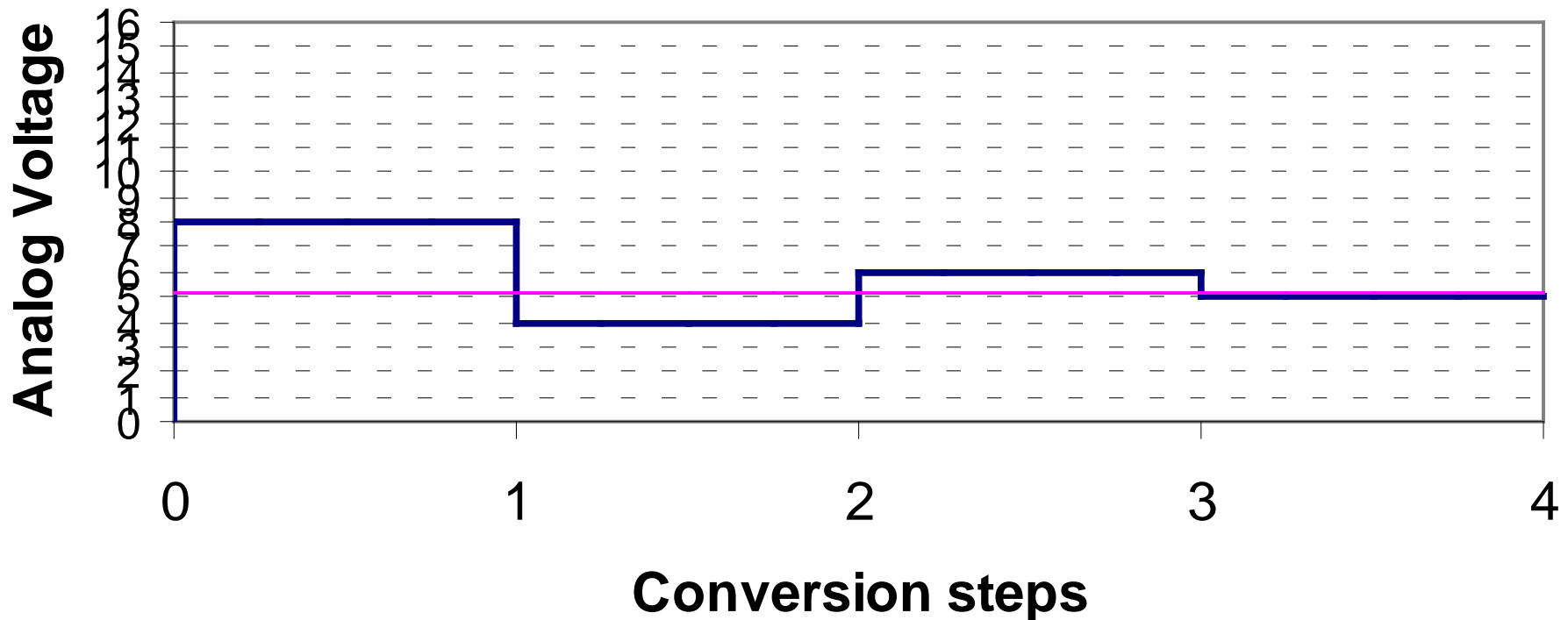
(a) MSB trial

(b) 2^2-bit trial

(c) 2^1-bit trial

(d) LSB trial (conversion complete)

Analog Voltage

16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0

0   1   2   3   4
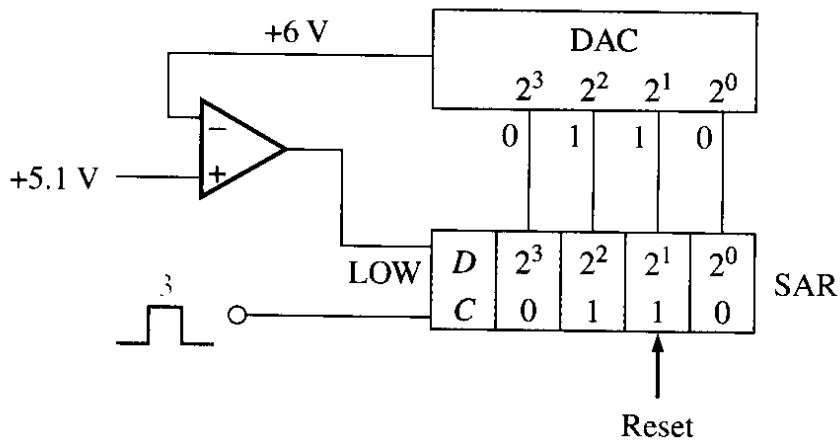
Conversion steps

— Reference Voltage   — Analog Input Voltage

Characteristic of the SAC process:

• The number of comparison steps that need to be done is always equal to the number of output bits in the converter. More bits will thus lead to better accuracy but also a slower conversion process.

• The time to perform a conversion process will always be the same for a particular converter

• This conversion speed is relatively fast compared to some other types of converters (eg. ramp converters) but not as fast as the high priced flash converters. Moderately priced.

Problem:

An eight-bit SAC has a resolution of 20 mV. What will its digital output be for an analog input of 2.17 V?

Solution:

2.17 V/20 mV = 108.5

so that step 108 would produce V_{AX} = 2.16 V and step 109 would produce 2.18 V.

The SAC always produces a final V_{AX} that is at the step below V_A.

Therefore, for the case of V_A = 2.17 V, the digital result would be

108_{10} = 01101100_2.